2021 科学技術英語 2 秋学期期末試験 STE210118_Exam.txt

[ ]年[ ]組[ ]番号 氏名[ ] 実施日[ ]年[ ]月[ ]日

問題 1(19) A~F 中 原文と合致するものに[1]、そうでないものに[0]を記入してください。

The datapath is the core of the processor; it is where all computations are performed. The other blocks in the processor are support units that store either the results produced by the datapath or help to determine what will happen in the next cycle.

A typical datapath consists of an interconnection of basic combinational functions, such as logic (AND, OR, EXOR) or arithmetic operators (addition, multiplication, comparison, shift). Intermediate results are stored in registers. The design of the arithmetic operators is the topic of this chapter. The control module determines what actions happen in the processor at any given point in time. A controller can be viewed as a finite state machine (FSM). It consists of registers and logic, and is hence a sequential circuit. The logic can be implemented in different ways—either as an interconnection of basic logic gates, often called random logic, or in a more structured fashion using programmable logic arrays (PLAs) and instruction memories.

A. [ ] データパスはプロセッサの中の中核的な機能である

B. [ ] データパスを構成する主要な機能には算術演算と論理演算がある

C. [ ] EXOR とは排他的論理和で、加算回路で主要な役割を果たす

D. [ ] FSM はデータパス回路の中でコアとなる役割を果たす

E. [ ] 基本ゲートの組み合わせはランダムロジックと呼ばれる

F. [ ] ロジックは PLA で構成されることもある

問題 2(19)次の文から各種メモリはどのような観点から分類されるかを要約してください。

The memory module serves as centralized data storage. A broad range of different memory classes exist. The main difference between those classes is in the way data can be accessed, such as read-only versus read-write, sequential versus random access, or single-ported versus multiported access. Another way of differentiating between memories is related to their data-retention capabilities. Dynamic memory structures must be refreshed periodically to keep their data, while static memories keep their data as long as the power source is turned on. Finally, memory structures such as flash memories conserve the stored data even when the supply voltage is removed. A single processor might combine different memory classes. For instance, random access memory can be used to store data and read-only memory to store instructions.

問題 3(19)次に示す Technical Term から 5 語以上を使用して選び 50 語以上の技術英文を作ってください。名詞や動詞の単複数、活用形などは文法に基づいて変化させてください。複数の文で構成してもかまいませんが、その場合は各文が内容的に繋がるように書いてください。用語の適切な使用と英文が正しくかけているかに留意してください。内容が物理科学的に誤っていても減点の対象にしません。

describe, consider, discuss, study, investigate, analyze, develop. focus, present, improve, explain, evaluate, provide, increase, outline, report, suggest, problem, paper, figure, CMOS, transistor, FET, channel, gate, current, voltage, power, consumption,

問題 4(21) (　)内に適当な冠詞を入れよ

6.2.3 Master-Slave and Edge-Triggered FFs

(　)JK flip-flop presented above is also called(　)latch. (　)flip-flop is(　)latch if the gate is transparent while the clock is high (low) [Hill74], Any change at the input is reflected at the output after(　)nominal delay. The latch is said to open with the rising of the clock. Data is accepted continuously until the clock goes down and the latch closes.

The transparent nature of the latch can cause some severe problems. Consider the simple circuit of Figure 6.7. As long as(　)clock is high, the output of the flip-flop oscillates back and forth between the 0 and the 1 states. This phenomenon is called(　)race (or race-around) condition and can only be avoided by making the pulse width of smaller than the propagation delay of the loop. Since the loop delay in the example is small, and probably smaller than the pulse width, this situation has(　)major chance of occurring. The result of this repetitive toggling is that(　)output is undetermined when the clock goes low. Observe that a JK flip-flop has(　)intrinsic race problem when J and K are high, as　discussed earlier.

書ききれない場合には、余白を使ってください。