# Science and Technology English II

# Exercise 208 “Flip-Flop” Meiji University 2020

EX_208.pptx 16 Slides September 24th.,2019

http://mikami.a.la9.jp/mdc/mdc1.htm


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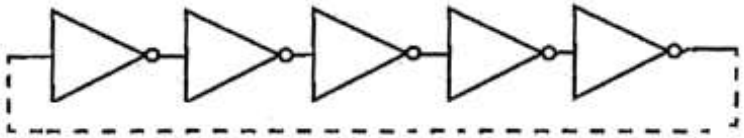
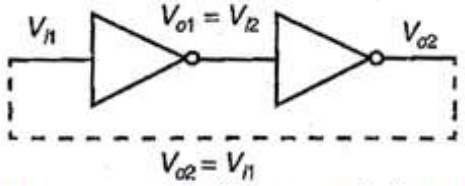
# Day 207 Review

- 近代のVLSI設計は、すべて完全同期式回路で構成する
- Ring Oscillator (Chapter3)や Cross coupled inverter (Chapter6)は基本的に設計ルール外 (理由:配置やレイアウト次第で特性が変わり、動作保証ができない)

- Set Up/Hold time が不足するとゲートのチャージが不十分となり出力が不安定になる
(メタステーブル : 準安定状態)

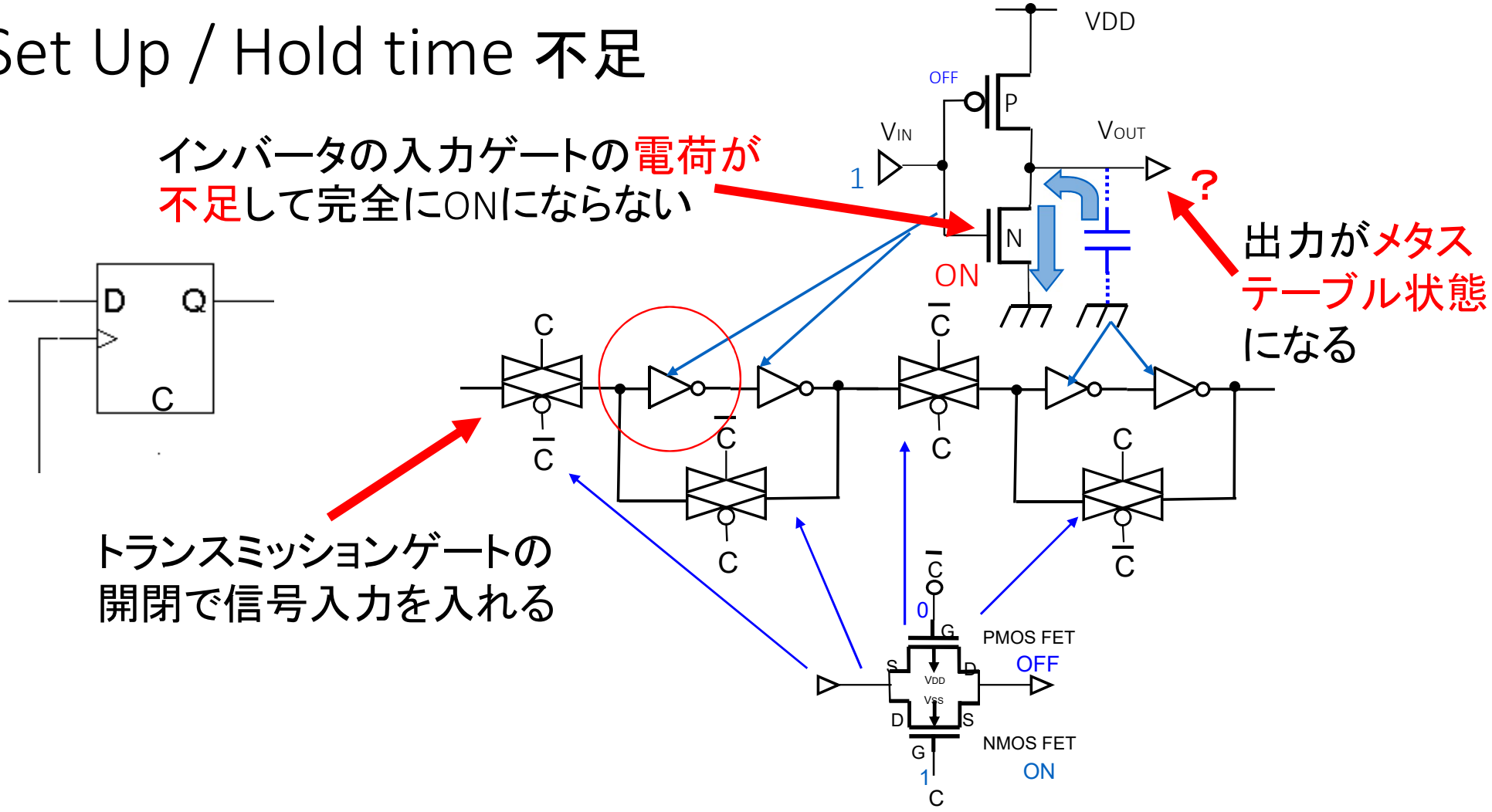


Ring Oscillator (Chapter3)

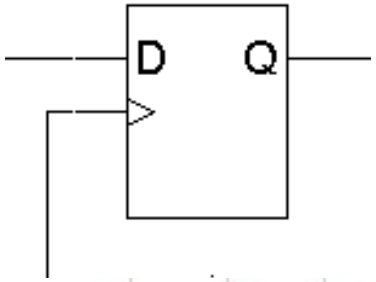



Cross coupled inverter (Chapter6)

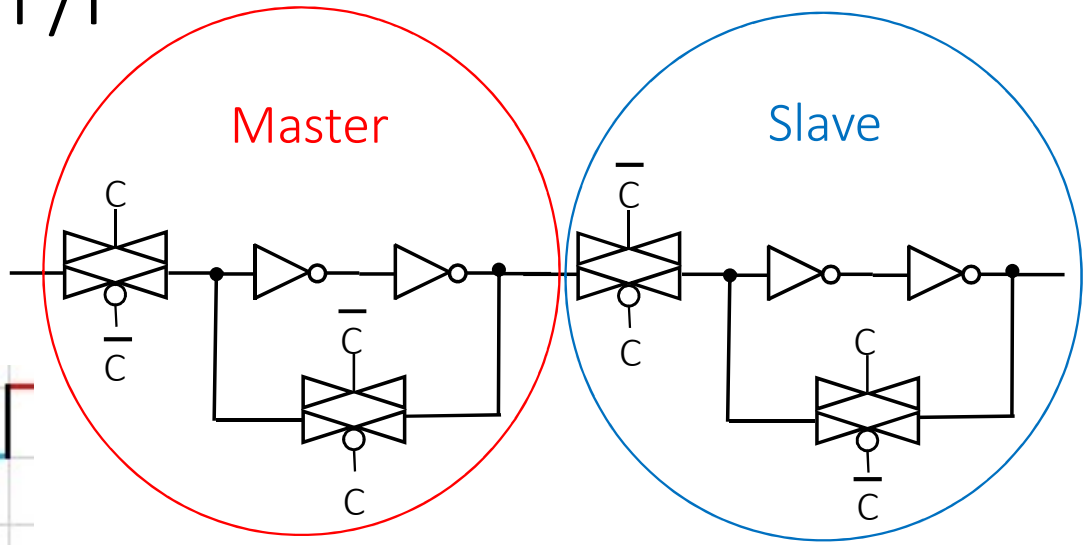
# Set Up / Hold time 不足



# D-type Master / Slave F/F




| | | | | | | |
|---|---|---|---|---|---|---|
| Clock | | T4 | T3 | T2 | T1 | |
| | | | | | | |
| DIN | D | C | C | B | B | |
| M T-Gate | | 閉 | 開 | 閉 | 開 | 閉 |
| M Latch | | C | C | B | B | — |
| | | | | | | |
| S T-Gate | | 開 | 閉 | 開 | 閉 | 開 |
| S Latch | | C | B | B | — | — |
| FF-OUT | | C | B | B | | |




Master側とSlave側の
トランスミッションゲートが
交互に開閉してデータを送りだす

# Day 208 Latch to Flip-Flop

- 論理回路は、2種類がある Combinational Logic と Sequential Logic
- Combinational Logic (組合せ回路)
  - $Fcout = f(In1, In2, ..InN)$
  - 出力が入力のみで(一意に)定まる
- Sequential Logic (順序回路)
  - $Fsout = f(Internal\_State, In1, In2, ..InN)$
  - 出力が入力と内部状態で(一意に)定まる
- 内部状態を保持する回路 – Flip Flop

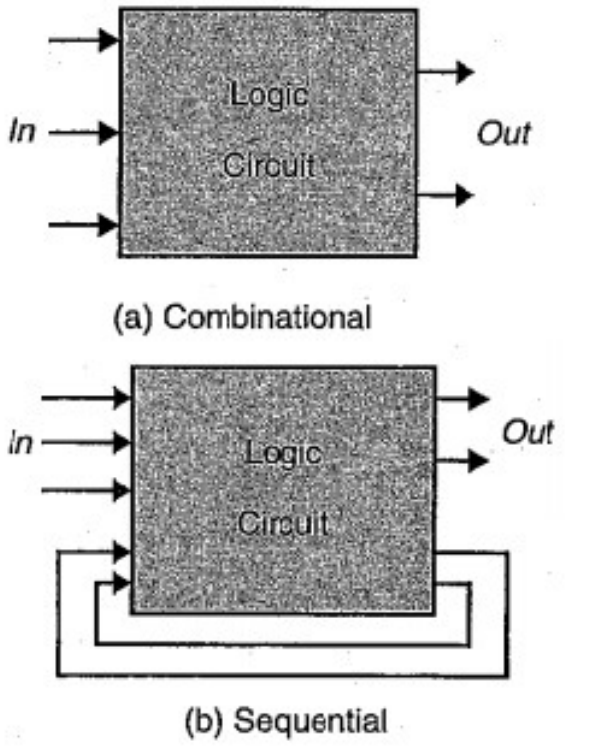
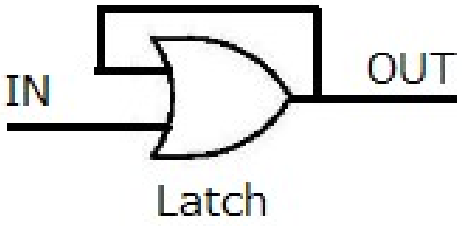



**Figure 4.1** Classification of logic circuits.

# Latch 閂(かんぬき)

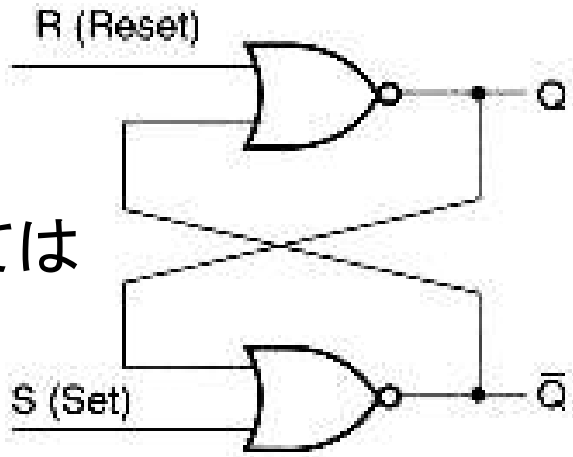
- もっとシンプルなラッチ-> いったん 1 になったらそのまま -> 1にセットするだけしかできない




- SR Latch

Set (1) とReset (0) ができるラッチ

しかし S と R が同時に 1 になってはいけない(禁止)




(a) Logic diagram

SR Latch

| S | R | Q | $\bar{Q}$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | Set state |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | Reset state |
| 0 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 0 | Undefined |

(b) Function table

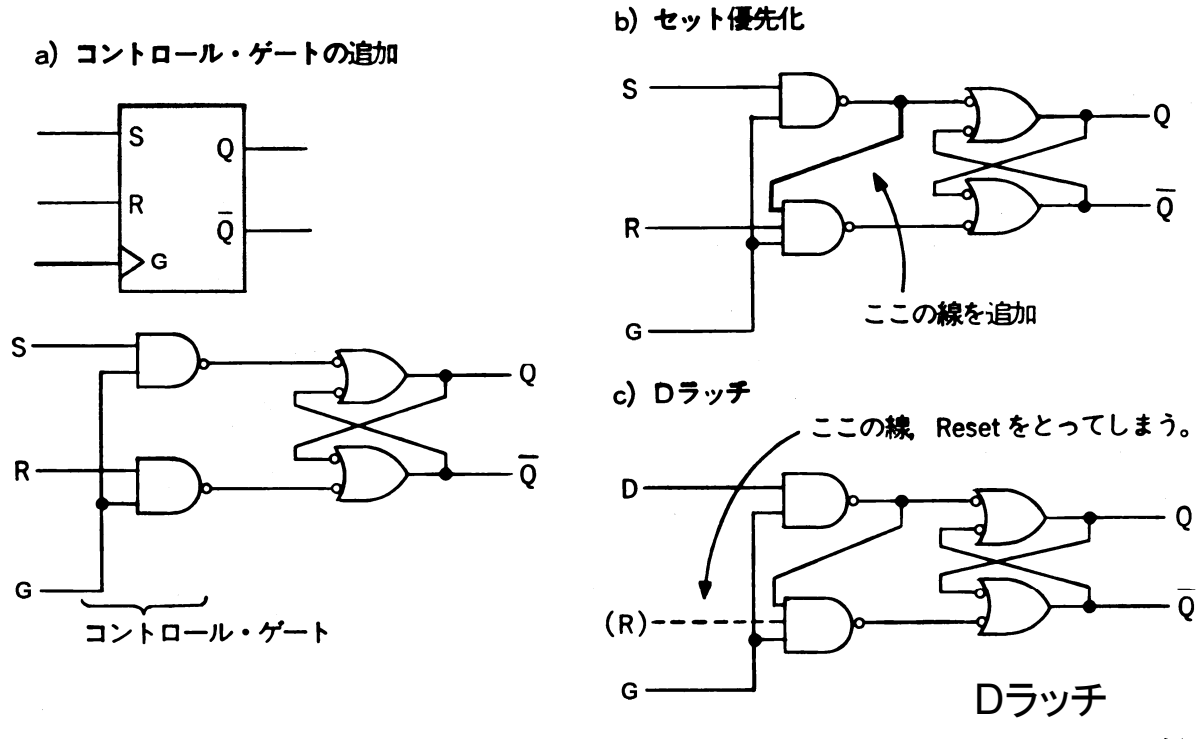
Latch は非同期動作をする

F/F は,Clock による同期動作をする

EX_208-1 と関係します。

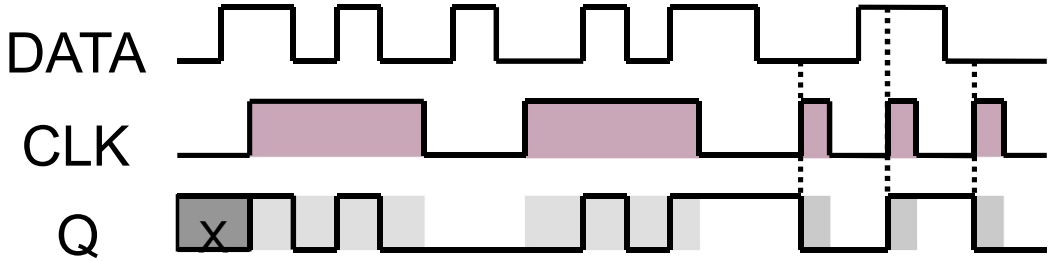
# SRラッチのアレンジ

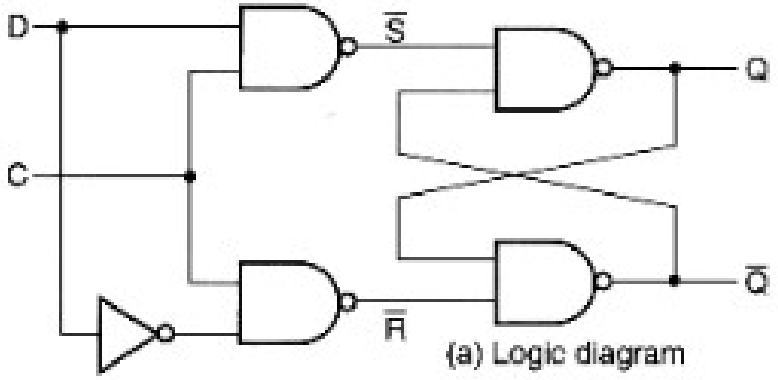
## コントロール・ゲート追加とセット優先化



# D Latch

- Control Gate を追加し、Gateが開いている間だけ内部状態が変化する
- 入力と出力が等しく、Cが開いていた前の状態を保持する。D はDelay を意味する



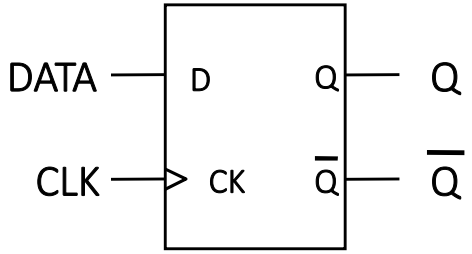

(a) Logic diagram

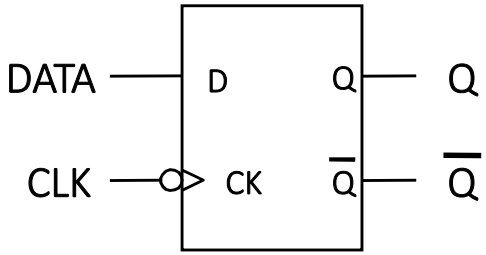
| C | D | Next state of Q |
|---|---|---|
| 0 | X | No change |
| 1 | 0 | Q = 0; Reset state |
| 1 | 1 | Q = 1; Set state |

(b) Function table

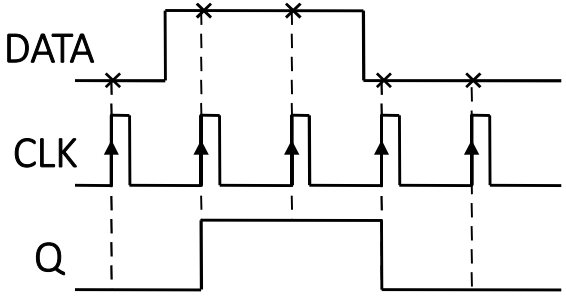
# D Flip-Fop

D端子に入力された信号をクロック信号のエッジに同期して保持し,
そのままQ端子に出力(クロックの立ち上がりと立ち下り同期の2種)

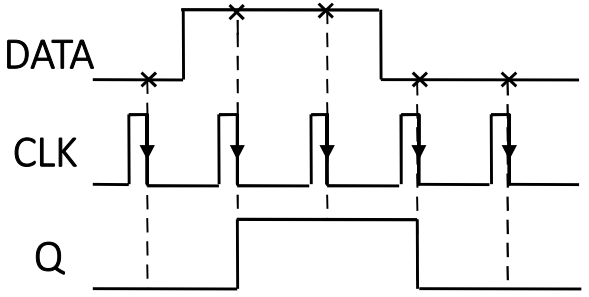


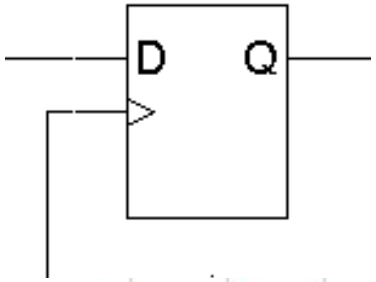

**クロックパルスの立ち上がりで動作**



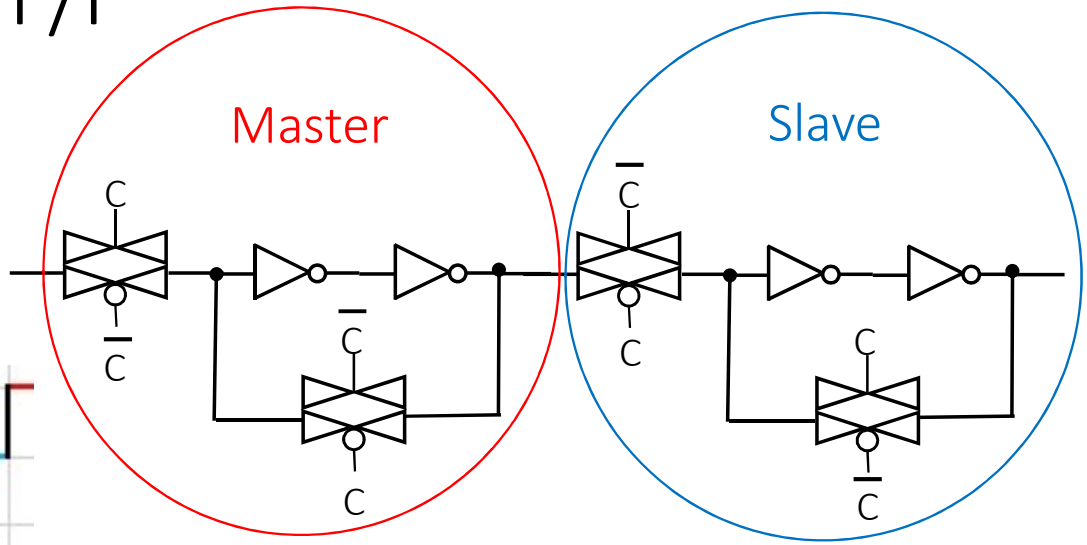

**クロックパルスの立ち下がりで動作**



# D-type Master / Slave F/F




| Clock | | T4 | T3 | T2 | T1 | |
|---|---|---|---|---|---|---|
| | | | | | | |
| DIN | D | C | C | B | B | |
| M T-Gate | | 閉 | 開 | 閉 | 開 | 閉 |
| M Latch | | C | C | B | B | — |
| | | | | | | |
| S T-Gate | | 開 | 閉 | 開 | 閉 | 開 |
| S Latch | | C | B | B | — | — |
| FF-OUT | | C | B | B | | |




Clock による同期動作をするCMOS F/F
Master側とSlave側が Clock で分離動作しているのでレーシングを回避できる

# Exercise: EX_208 文意をつかむ

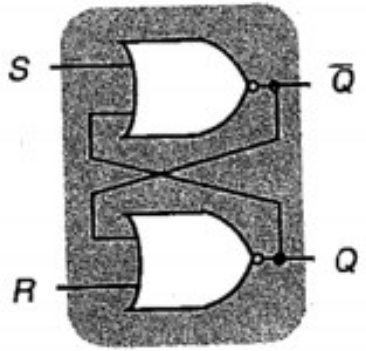
- 本文の以下のページを速読し設問に和文または英文で答えよ。翻訳サイトを使ってもよいが、その前に必ず英文を通読すること。)図版や正確なギリシャ文字,数式は配布資料原本を参照のこと。
- EX_208-1 : P335 STE-102-603 Line 21 ~ P336 STE-102-604 Line 8まで
  - 6.2.2 Flip-Flop Classification
  - 原本で言及している内容を考慮して、Figure 6.3 の図版の修正すべき点とその理由を指摘せよ。
- EX_208-2 : P338 STE-102-606 ~ Line 28 まで
  - 6.2.3 Master-Slave and Edge-Triggered FFs
  - 原本で言及している “latch の問題点” とは何か、その解決の方法と原理はどのようなものか、原本で取り上げている回路の動作を考察すること。
- 提出はClass Web Report水曜まで

# EX_208-1(1) : P335 STE-102-603 Line 21 ~

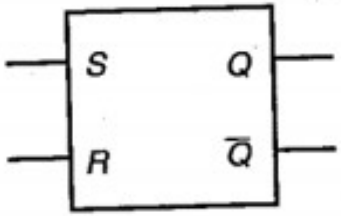
- 6.2.2 Flip-Flop Classification
- In the logic design world, a number of different flip-flop (FF) types are known. The simplest one is the SR flip-flop (or set-reset flip-flop). One possible implementation, using only NOR gates, is shown in Figure 6.3a. The logic symbol for this circuit is given in Figure 6.3b. This circuit is similar to the cross-coupled inverter pair with the inverters replaced by NOR gates. The second input of the NOR gates is connected to the trigger inputs (S and R), which makes it possible to force the outputs Q and O to a given state. These outputs are complimentary. When both S and R are 0, the flip-flop is in a quiescent state and both outputs retain their value. If a positive (or 1) pulse is applied to the S input, the Q output is forced into the 1 state (with O going to 0), Vice versa, a 1 pulse on R resets the flip-flop and the Q output goes to 0. The length of the trigger pulse has to be larger than  the loop delay of the cross-coupled pair, as we have already noted.
- Figure 6.3 NOR-based SR flip-flop. (Continue to next page)

# EX_208-1(2) : P336 STE-102-604 Line 8まで

Figure 6.3 NOR-based SR flip-flop.




(a) Schematic diagram




(b) Logic symbol

| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |

(c) Characteristic table

- The SR flip-flop can also be implemented with NAND gates, as shown in Figure 6.4. As we can deduce from the circuit diagram and the characteristic table, the quiescent state of the latch corresponds to both S and R high. A negative-going (or O) pulse on S or R respectively sets or resets the flip-flop. Having both S and R equal to zero is forbidden. The small circles at the inputs of the NAND-gate SR flip-flop indicate that the gate is triggered by a negative-going pulse, or operates on so-called negative logic. This is in contrast with the NOR-based FF, which triggers on positive-going pulses, and is therefore said to operate on positive logic.

# EX_208-2(1): P338 STE-102-606 ~ Line 14 まで

- 6.2.3 Master-Slave and Edge-Triggered FFs
- The JK flip-flop presented above is also called a latch. A flip-flop is a latch if the gate is transparent while the clock is high (low) [Hill74], Any change at the input is reflected at the output after a nominal delay. The latch is said to open with the rising of the clock. Data is accepted continuously until the clock goes down and the latch closes.
- The transparent nature of the latch can cause some severe problems. Consider the simple circuit of Figure 6.7. As long as the clock is high, the output of the flip-flop oscillates back and forth between the 0 and the 1 states. This phenomenon is called a race (or race-around) condition and can only be avoided by making the pulse width of smaller than the propagation delay of the loop. Since the loop delay in the example is small, and probably smaller than the pulse width, this situation has a major chance of occurring. The result of this repetitive toggling is that the output is undetermined when the clock goes low. Observe that a JK flip-flop has an intrinsic race problem when J and K are high, as discussed earlier.

# EX_208-2(2): P338 STE-102-606 Line 15~ Line 28 まで

One way to avoid a race is to use the master-slave approach. Master-slave flip-flops are built by cascading two basic flip-flops with opposite clock phases, as illustrated in Figure 6.8. The first flip-flop, called the master, becomes operational when the clock goes high. During this period, inputs J and K are enabled, and the intermediate signals SI and RI can be changed. The feedback of the Q and notQ signals ensures that the flip-flop acts as a JK flip-flop that toggles when both J and K are high. The not φ clock is low in this time period, putting the second FF, called the slave, in the hold mode. This prevents the changes in SI and RI from propagating to the Q and O outputs. On the falling edge of the clock, φ goes down, freezing the state of the master latch. A very short time later, the NAND input gates of the slave latch are enabled, and the changes in SI and RI are propagated to the outputs. Due to this master-slave operation, there is no limitation on the width of the clock pulse, since the master latch is disabled at the time the outputs are changing, and no racing around can occur. In other words, the master-slave principle makes sure that the feedback path of the flip-flop is always interrupted either at the master or slave side. The pulse lengths of φ and not φ have to be larger than the propagation delays of the master (slave) latches for this structure to be functional.

# Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

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