Science and Technology English II

Exercise 205 “CMOS3” Meiji University 2020

EX_205.pptx 14 Slides October 19th.,2020

http://mikami.a.la9.jp/mdc/mdc1.htm

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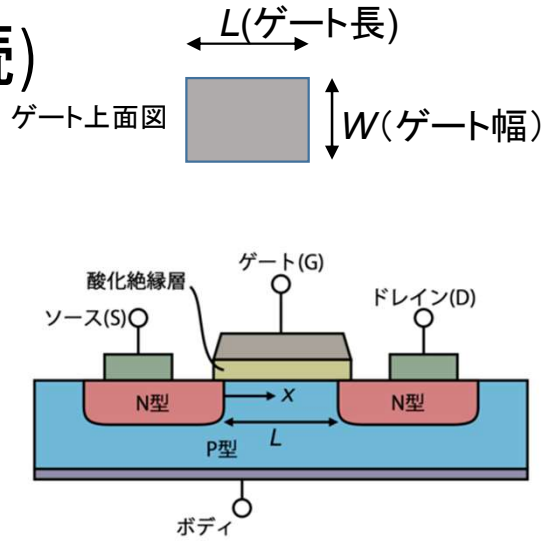
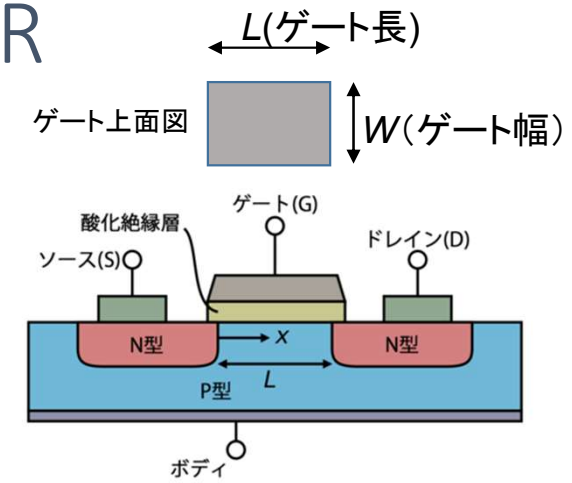
Day 204 Review : CMOS Technology

- CMOS / FET
- CMOS回路(P/Nチャネル半導体を相補接続)
- MOS FET
- CMOS Inverter 回路とPUP / PDN
- CMOS インバータ回路
- インバータ回路とNAND/NOR化
- CMOS 多入力ゲート

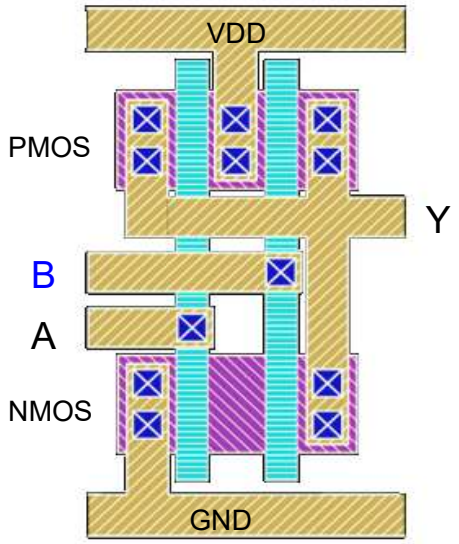


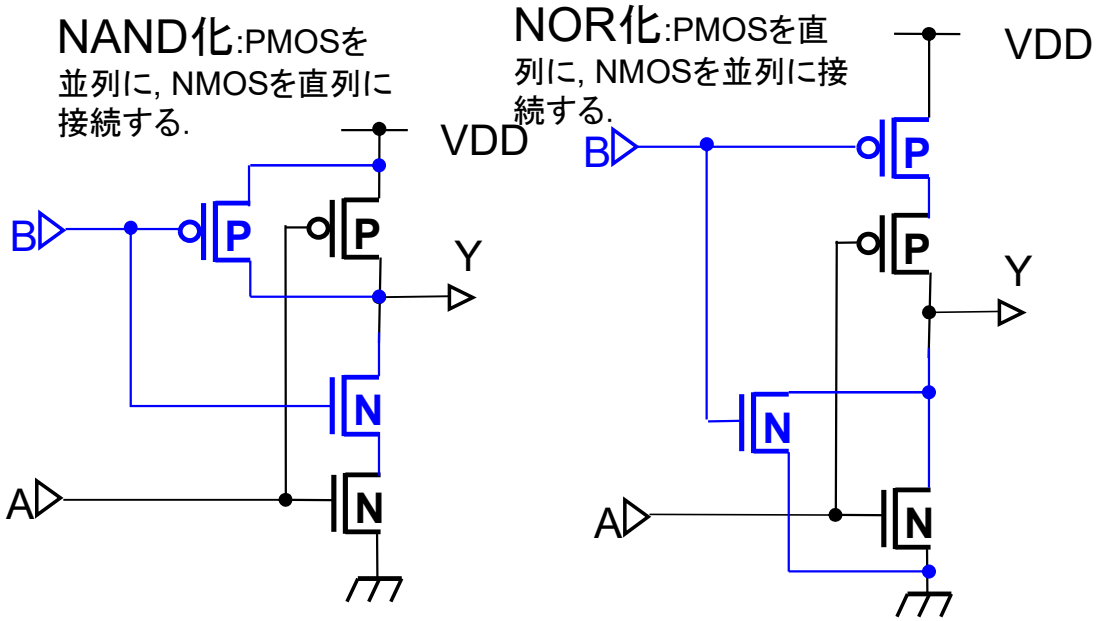
Day 204 Review: Inverter to NAND/NOR

P200 : Example 4.5 STE-102-405 上図のLがゲート長で、この最小値がプロセスルール(例:L=90nm, 90nmプロセス)
Wがゲート幅で　W/L が重要な特性指標になる。

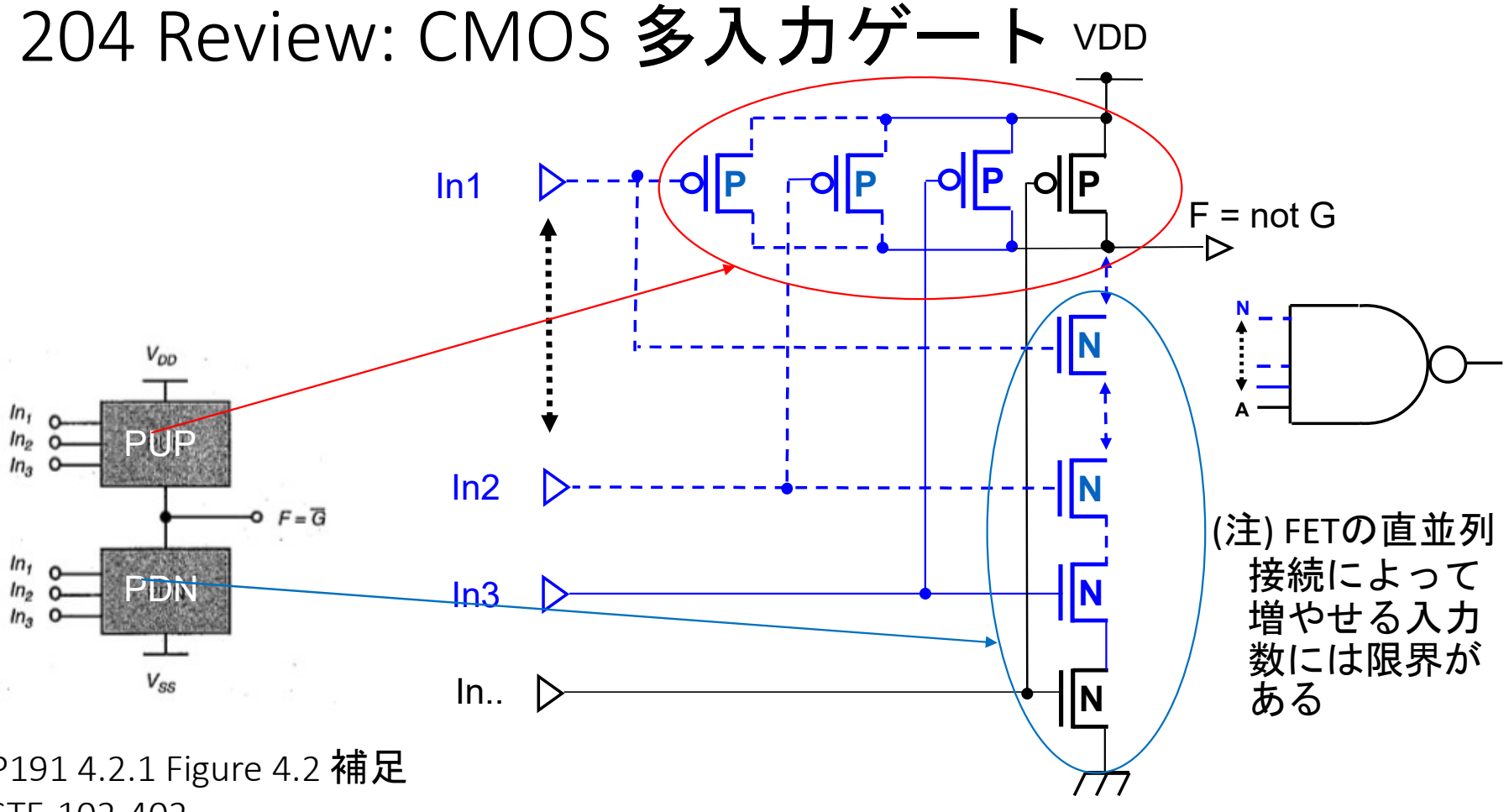


NAND 回路のレイアウト



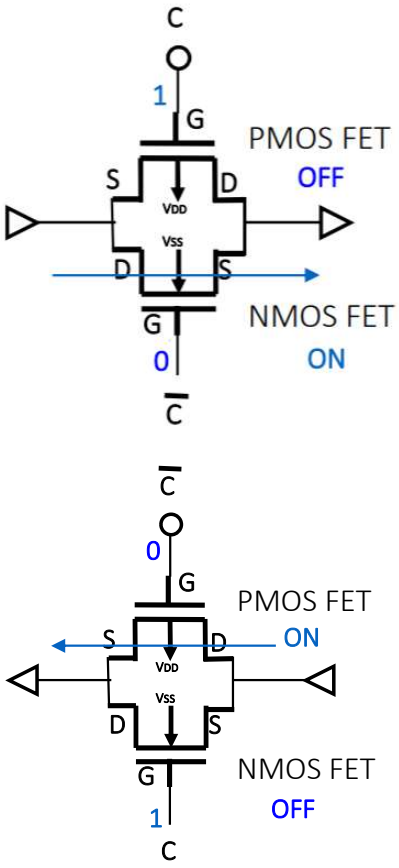


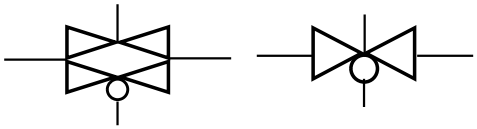
Day 204 Review: CMOS 多入力ゲート



P191 4.2.1 Figure 4.2 補足
STE-102-402

Transmission Gate





記号

PMOS FET とNMOS FETを接続したトランスファー(伝達)ゲート

双方向で動作するアナログ・スイッチ

オン抵抗は高い

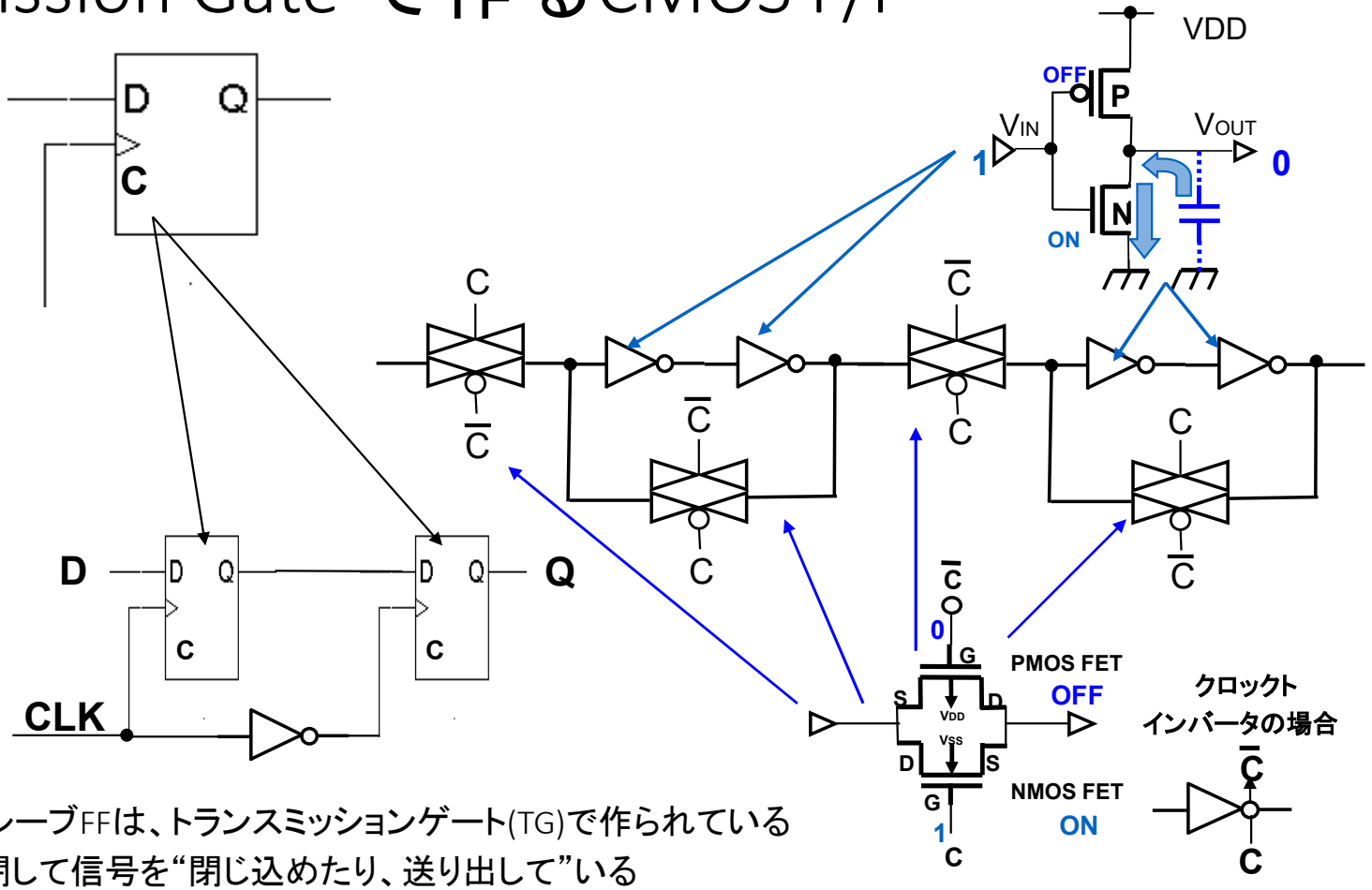
回路の開閉に使用される

FPGAの配線部やF/Fに使われる

P212 STE-102-407
Figure 4.22
P213 STE-102-408

Transmission Gate
の解説

Transmission Gate で作るCMOS F/F



CMOS マスタースレーブFFは、トランスミッションゲート(TG)で作られている
TG は、交互に開閉して信号を“閉じ込めたり、送り出して”いる

Transmission Gate XOR

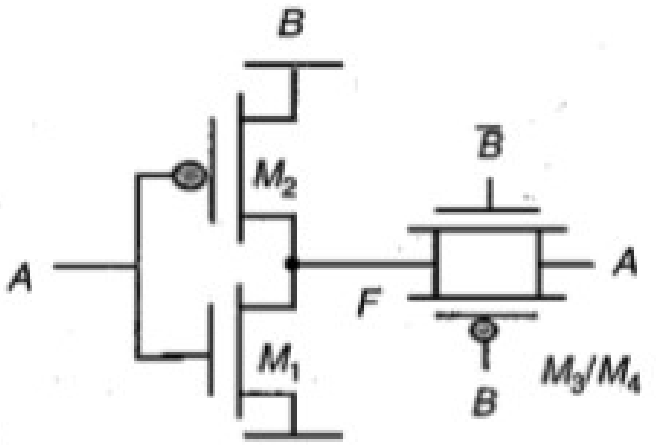
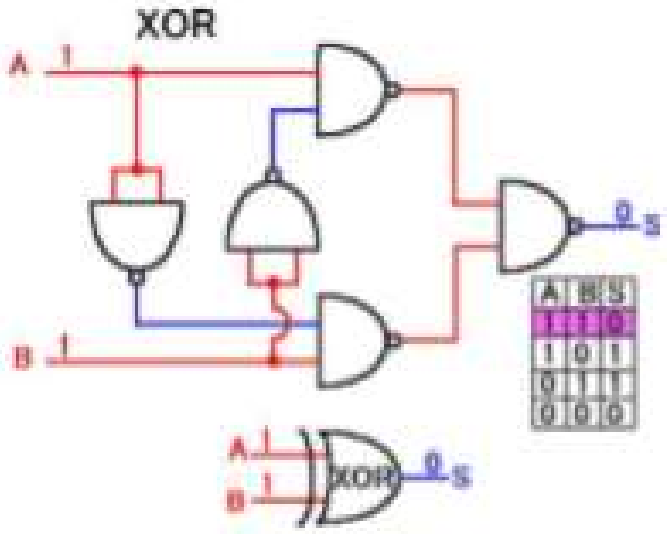


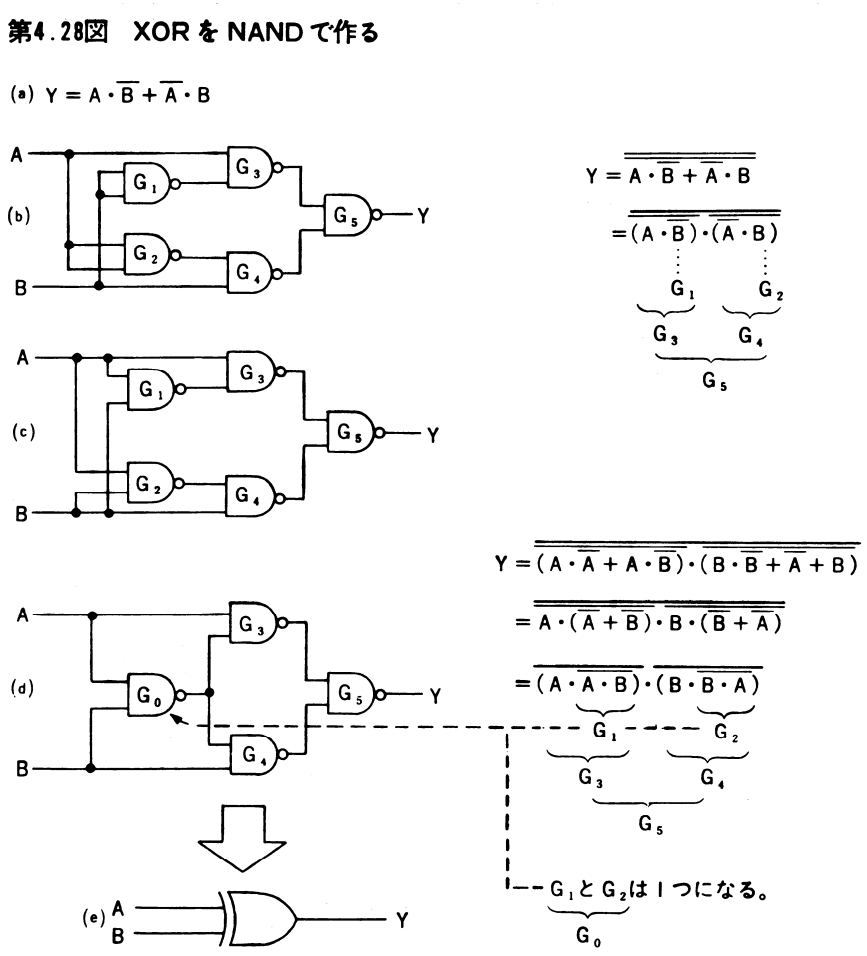
Figure 4.23 Transmission gate XOR.



P213 STE-102-408
Figure 4.23

Transmission Gate
XORの解説

TANT回路 NAND またはNOR の3段で任意回路を実現



- ユニバーサル演算(子)
- NAND / NOR
- PLA (Sum Of Product)

Exercise: EX_205 文意要約

- 本文の以下のページを速読し、文意を要約して日本語でまとめる。
- 和文翻訳サイトを使ってもよいが、その前に必ず英文を通読すること。
- 図版や正確なギリシャ文字,数式は配布資料原本を参照のこと。
- EX_205-1 : P212 Line 14~ Transmission gates can be~ 4.2 STE-102-407
  - Transmission gates can be used to build some complex gates very efficiently.
- EX_205-2 : P212 Bottom 5lines: Another example ~ P213 Line 10まで
  - Another example of the effective use of transmission gates ~ Figure 4.23
- EX_205-3 : P213 Line 11 ~ 30まで STE-102-408
  - Design Issues in Static Pass-Transistor Logic Design
- 提出はClass Web Report水曜まで

EX_205-1 :P212 Line 14~ Transmission gates can be~ 4.2 STE-102-407

- Transmission gates can be used to build some complex gates very efficiently. The simplest example of this type of circuit is the (inverting) two-input multiplexer shown in Figure 4.22. This gate either selects input A or B based on the value of the control signal S, which is equivalent to implementing the following Boolean function:
- $$\text{not } F = (A \cdot S + B \cdot \text{not } S) \qquad (4.15)$$
- A complementary implementation of the gate requires eight transistors instead of six.
- Figure 4.22 Transmission gate multiplexer and its layout.

EX_205-2 : Another example of the effective use of transmission gates

STE-102-407 ~ 408

- Another example of the effective use of transmission gates is the popular XOR circuit shown in Figure 4.23. The complete implementation of this gate requires only six transistors (including the inverter used for the generation of not b), compared to the twelve transistors required for a complementary implementation. To understand the operation of this circuit, we have to analyze the B = 0 and B = 1 cases separately. For B = 1, transistors M1 and M2 act as an inverter while the transmission gate M3/M4 is off; hence F = (not A) and B. In the opposite case, M1 and M2 are disabled, and the transmission gate is operational, or F = A and (not B). The combination of both results in the XOR function. Notice that, regardless of the values of A and B, node F always has a connection to either VDD or GND and is hence a low-impedance node. If this were not true, the circuit would be dynamic, and an occasional refresh would be required to counter the effects of charge leakage. When designing static-pass transistor networks, it is essential to adhere to the low-impedance rule under all circumstances. Other examples where transmission-gate logic is effectively used are fast adder circuits and registers. Both circuits will be discussed in later chapters.

EX_205-3(1) : Design Issues in Static Pass-Transistor Logic Design

STE-102-408

Design Issues in Static Pass-Transistor Logic Design

- When designing transmission-gate-based devices, one has to be aware of a number of design problems that are specific to that circuit class.
- 1. Resistance.
- A transmission gate is, unfortunately, not an ideal switch, because it has a series resistance associated with it. To get an idea of the nature and value of this resistance, let us analyze the design instance of Figure 4.21c, when charging a capacitance CL from 0 V to VDD, that is, when passing a 1 from input to output. The resistance of the switch is modeled as a parallel connection of the resistances Rn and Rp of the NMOS and PMOS devices, defined as (VDD - Vout)/In and (VDD - Vout)/Ip, respectively, The currents through the devices are obviously dependent on the value of Vout and the operating mode of the transistors.

EX_205-3(2) : Continued - Design Issues in Static Pass-Transistor Logic Design

STE-102-408

- During the low-to-high transition, the pass-transistors traverse through number of operation modes. As its VGS is always equal to VDS, the NMOS transistor is either in saturation or off. The VGS of the PMOS is equal to VDD, and the device changes from saturation to linear during the transient. When computing Ip and In, it is important to incorporate the body effect. The operating modes of the transistors for different ranges of Vout are summarized below.
- Vout< |VTp|: NMOS and PMOS saturated.
- |VTp| < Vout < VDD-VTn: NMOS saturated, PMOS linear.
- VDD - VTn < Vout : NMOS cutoff, PMOS linear.

Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

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