Science and Technology English II

Exercise 204 “CMOS2” Meiji University 2020

EX_204.pptx 13 Slides September 24th.,2019

http://mikami.a.la9.jp/mdc/mdc1.htm

Renji Mikami

Renji_Mikami(at_mark)nifty.com [mikami(at_mark)meiji.ac.jp]

Day 203 Review

- Complementary Metal oxide Semiconductor
- CMOS回路(P/Nチャネル半導体を相補接続)
- MOS FET
- 信号強度(ストレングス)
- CMOS Inverter 回路とPUP(Pull Up) / PDN(Pull Down)
- インバータ回路とNAND/NOR化

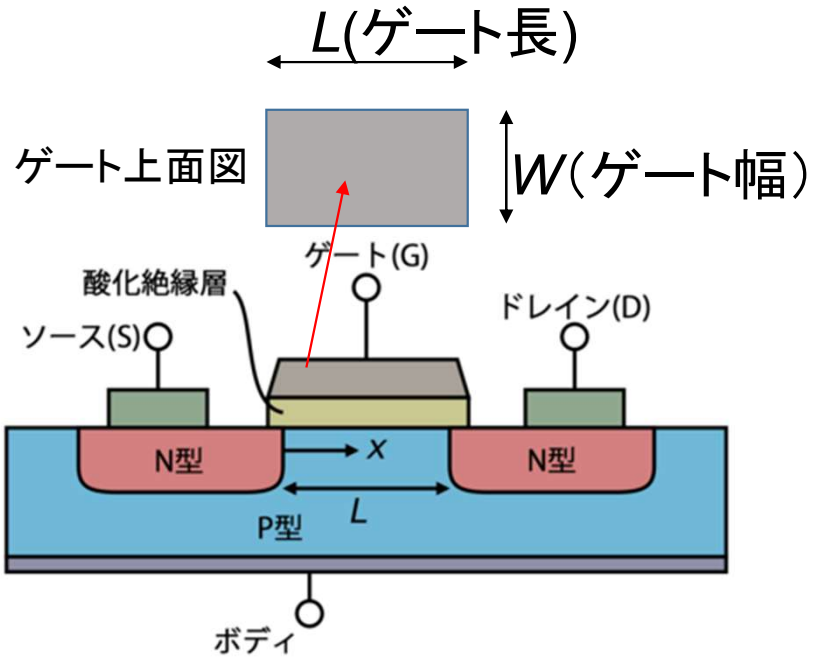
MOS FET

ゲート・ソース間電圧 V_{GS} を変化させるとドレイン電流 I_D が変化する。

N チャンネルタイプは、V_{GS}が高くなるとI_Dが増加する(エンハンスメント型)

P チャンネルタイプは、V_{GS}が高くなるとがI_D減少する(デプレッション型)

N 型と P 型を組み合わせた回路が CMOS(Complementary MOS)

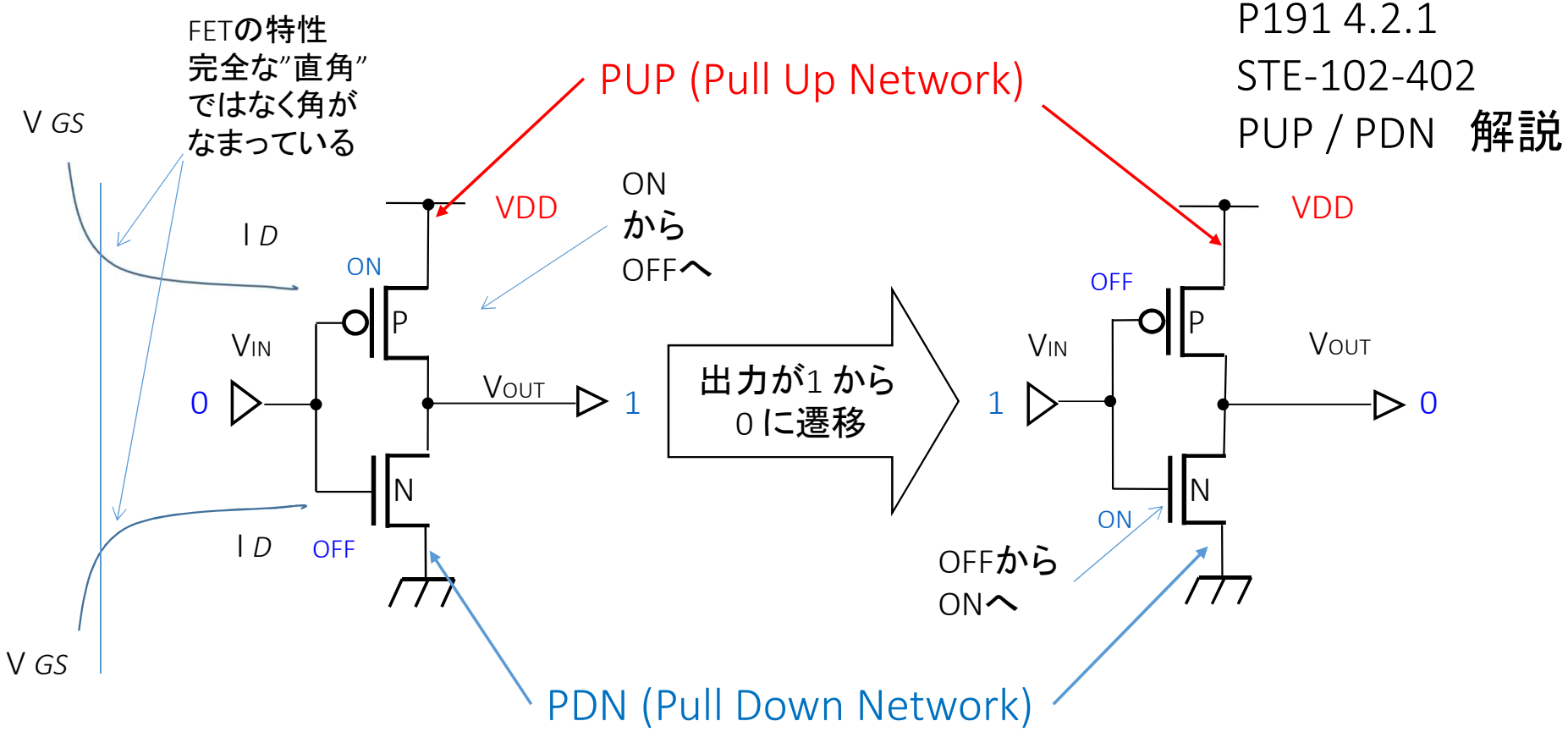


P200 : Example 4.5 STE-102-405 上図のLがゲート長で、この最小値がプロセスルール(例:L=90nm, 90nmプロセス)
Wがゲート幅で W/L が重要な特性指標になる。

トランジスタ 回路との比較
トランジスタでは、I_B ベース電流(ベース・エミッタ電流)でI_C コレクタ電流(コレクタ-エミッタ)が変化する。この比がh_{FE} 直流電流増幅率

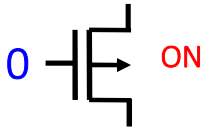
図版引用:ウィキペディア https://ja.wikipedia.org/wiki/MOSFET

CMOS Inverter 回路とPUP / PDN

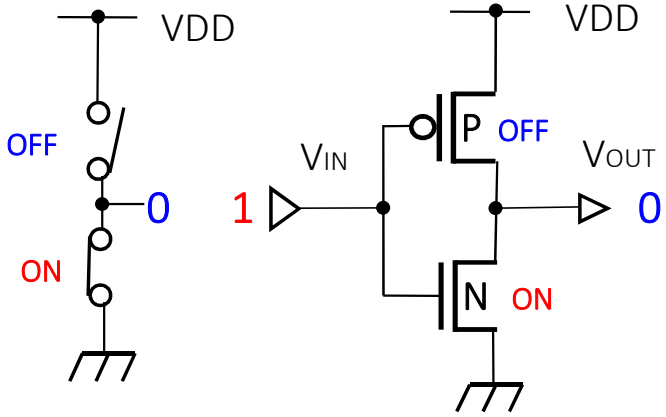


CMOS インバータ回路

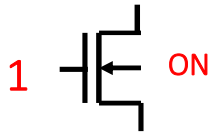
PMOS FET



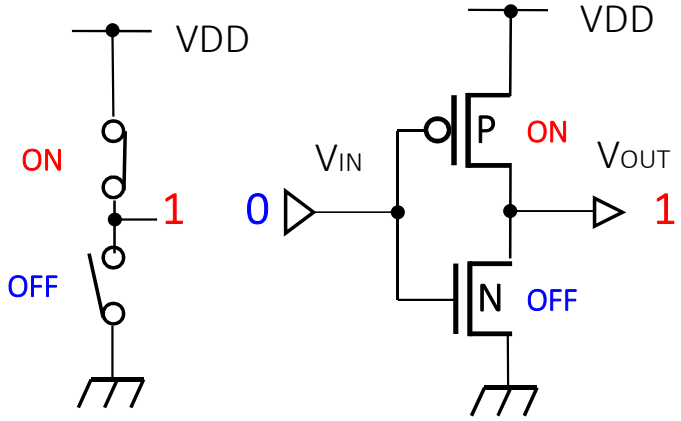
Vinが1のときは，PMOSがOFF, NMOSがON.
よってVOUTは0になる.



NMOS FET



Vinが0のときは，PMOSがON, NMOSがOFF.
よってVOUTは1になる.



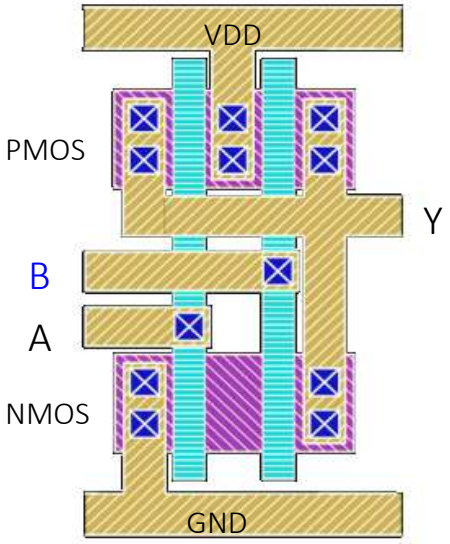
春学期 Review

- CMOS 回路はスイッチングした時に電流が流れる
- スイッチングしていないときはほとんど電流が流れない

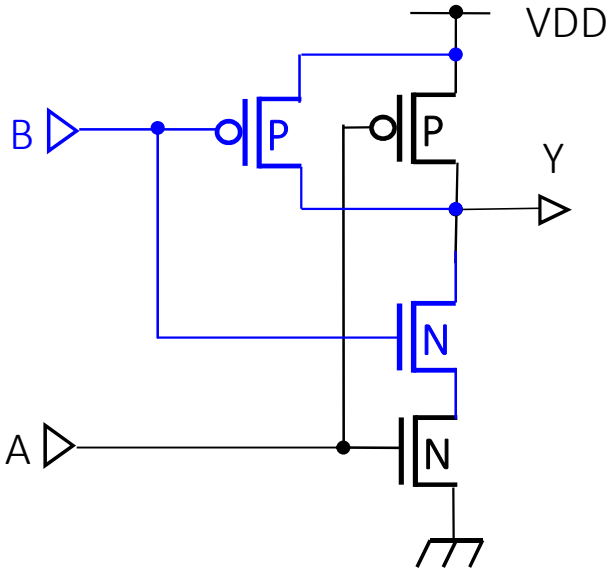
- トランジスタ回路では電流が流れ続ける
- そのため動作速度が遅いときはCMOSが低消費電力になる

インバータ回路とNAND/NOR化

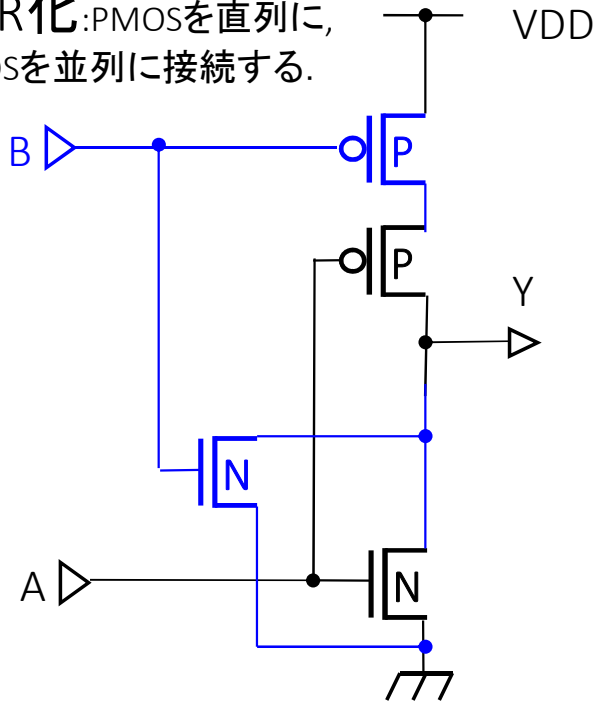
NAND 回路のレイアウト



NAND化:PMOSを並列に,
NMOSを直列に接続する.

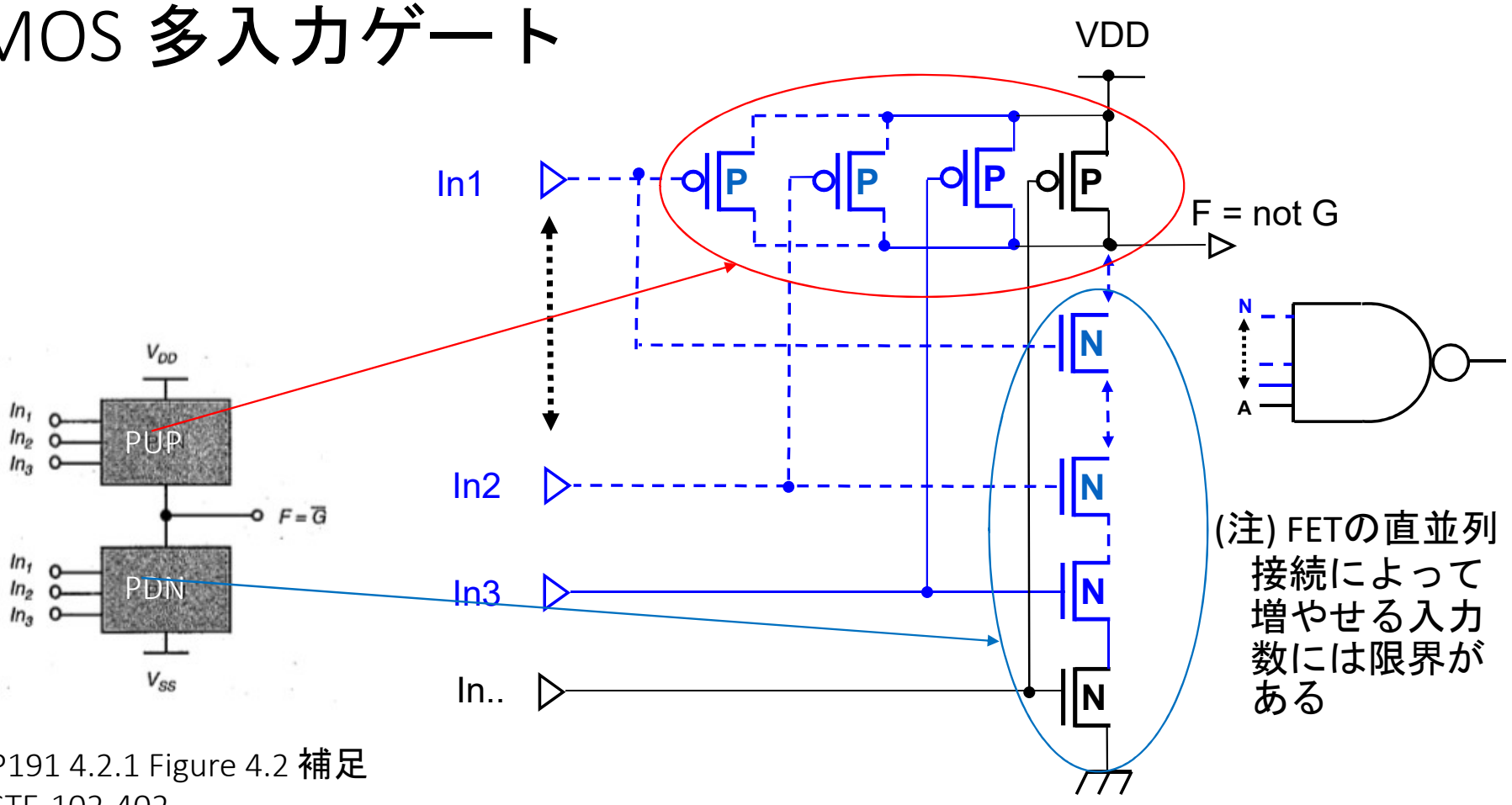


NOR化:PMOSを直列に,
NMOSを並列に接続する.



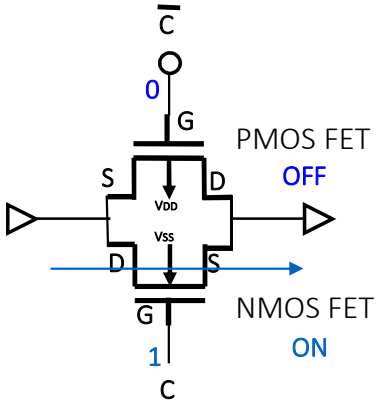
NANDとNORでは, ドライブ段の回路が違うので特性が異なる.

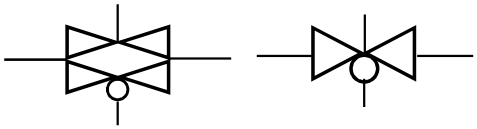
CMOS 多入力ゲート



P191 4.2.1 Figure 4.2 補足
STE-102-402

Day 205 Preview : Transmission Gate

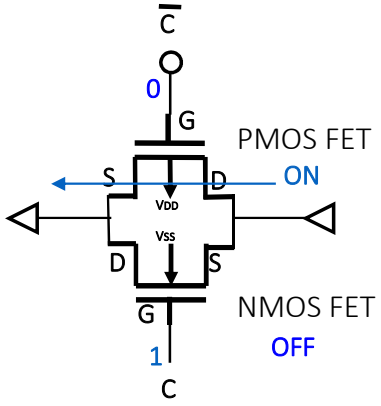




記号

P212 STE-102-407
Figure 4.22
P213 STE-102-408

Transmission Gate
の解説



PMOS FET とNMOS FETを接続したトランスファー(伝達)ゲート

双方向で動作するアナログ・スイッチ

オン抵抗は高い

回路の開閉に使用される

FPGAの配線部やF/Fに使われる

Exercise EX_204 文意要約

- 本文の以下のページを速読し、文意を要約して日本語でまとめる。
- 和文翻訳サイトを使ってもよいが、その前に必ず英文を通読すること。
- 図版や正確なギリシャ文字,数式は配布資料原本を参照のこと。
- EX_204-1 : P192 STE-102-403 Line16~28
- EX_204-2 : P192 STE-102-403 Line28 ~ P193 Figure 4.3まで

- 提出はClass Web Report水曜まで

EX_204-1 P192 STE-102-403 Line16~28

- A series connection of switches corresponds to an AND-operation, and a parallel connection of switches is equivalent to an OR-ing of the inputs.
- The pull-up and pull-down networks are dual networks, which means that a parallel connection of transistors in the pull-up network corresponds to a series connection of the corresponding devices in the pull-down network and vice versa.#1

- This property is understood from the following argument. Suppose that the pull down network of a CMOS gate is known and implements the logic function G. Since the PDN connects to GND, the CMOS gate implements the inverse function F = not G. We wish to derive the structure of the corresponding PUN. Since the PUN connects to VDD, it has to be conducting when F = TRUE (or in other words, it must implement F). Taking into account the above, as well as the fact that the PMOS transistors of the PUN are inverse switches, the following relation has to be valid:
- (not(G(ln1, In2, In3,…)) = F(not ln1, not In2, not In3…) (4.1)

EX_204-2 P192 STE-102-403 Line28 ~ P193 Figure 4.3まで

- This condition is met if (but not only if) F and G are dual equations, where each AND operation in F is replaced by an OR in G and vice-versa. This is a direct consequence of De Morgan's theorems, which state the following identities:
- not(A+B) = notA * notB, not A*B = notA + notE (4.2)
- The complementary gate is inverting (implementing functions such as NAND, NOR, and XNOR). Implementing a noninverting Boolean function (such as AND OR, or XOR) in one stage is not possible and requires the addition of an extra inverter stage.
- #1 The duality is a satisfying but not necessary requirement. Other valid PUN/PDN combinations can be envisioned, some of which will be illustrated in later chapters.
- Example 4.1 Two-input NAND Gate
- Figure 4.3 shows a simple two-input NAND gate (F = not (AB)). The PUN consists of two parallel PMOS transistors. This means that F is 1 if A = 0 or B = 0, which is equivalent to F= notA + notB = not (AB). The PDN, which consists of two series NMOS transistors, provides a connection to GND when both A=1 and B=1, Consequently, it implements G= AB = not F, which is consistent with the PUN network. It can be easily verified that the output F is always connected to either VDD or GND, but never to both.
- Figure 4.3 Two-input NAND gate in complementary static CMOS style.

EX_204-3 P200 STE-102-405 Line7 ~ Line 20まで

- Example 4.5 A Four-Input Complementary CMOS NAND Gate
- The layout of a four-input NAND gate is shown in Figure 4.10. No transistor sizing (besides the appropriate scaling of the PMOS devices for mobility) is applied. Hence all NMOS transistors have a (W/L) of (1.8/1.2), while the PMOS devices are set to (5.4/1.2).
- To simplify the manual analysis, it is customary to replace the serial chain of NMOS transistors by a single device whose channel length is the sum of the lengths of the transistors in the chain. This is equivalent to stating that the resistance of the discharge network is similar to the series connection of the resistances of the individual transistors. The parasitic capacitances of this hypothetical transistor. can be estimated as the sum of the capacitances of the individual devices (this is a worst-case scenario). Remember, however, that the merging of the series transistors into a single device is simplification that ignores a number of second-order influences, such as the body effect and the distributed nature of the parasitic capacitors.
- Figure 4.10 Layout and schematics of a four-input NAND gate in complementary CMOS. See also Colorplate 7.

Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

担当講師

三上廉司(みかみれんじ)

Renji_Mikami(at_mark)nifty.com

mikami(at_mark)meiji.ac.jp (Alternative)

http://mikami.a.la9.jp/_edu.htm