Science and Technology English I

Exercise 113 Meiji University 2020

(DICS Chapter-3 , Ring Oscillator)

EX_113.pptx 12 Slides November 24th.,2019

http://mikami.a.la9.jp/mdc/mdc1.htm

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Exercise: EX_113

- EX_113-1 から 3 を通読して和文または英文で要旨をまとめる。
- 自動翻訳は、課題文ごとに表示してある。

提出は、Class　Webで水曜まで

自動翻訳は、excite (https://www.excite.co.jp/world/english/) を使用

Day 14 試験について

EX_113-1 p117 [STE-101-309]

通読して和文または英文で要旨をまとめてください

The propagation delay of a gate is, a function of its fan-in and fan-out. Fan-out gates present an increased load (mostly capacitive) to the driving gate and slow its performance. The increased complexity of a gate due to a large fan-in also has a negative influence on the performance. When comparing the performance of gates in different technologies, it is important not to confuse the picture by including second-order parameters such as fan-in and fan-out. It is therefore useful to find a uniform way of measuring the tp of a gate, so that technologies can be judged on an equal footing. The de-facto standard circuit for delay measurement is the ring oscillator, which consists of an odd number of inverters connected in a circular chain (Figure 3.11). Due to the odd number of inversions, this circuit does not have a stable operating point and oscillates.

1 The 50% definition is inspired the assumption that the switching threshold VM is typically located in the middle of the logic swing.

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the 10% and 90% points of the waveforms (Figure 3.10).

デファクト標準

発振器

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発振する

EX_113-1 p117 [STE-101-309] 自動翻訳

ゲートの信号伝播時間はファンインとファンアウトの機能である。ファンアウトゲートは、ドライブゲートおよび遅さ そのパフォーマンス に、増大したロード（たいてい、静電容量である）を示す。大きいファンインによるゲートの増大したcomplexcityは、性能へのネガティブな影響も持っている。種々のテクノロジーのゲートの性能を比較する時には、写真を、ファンインやファンアウトなどの二番目注文パラメータを含むことと混同しないことが重要である。従って、ゲートのtpを測定するための均一な方法を見つけることが有益である。対等の立場でテクノロジーが判断されうるように。遅延測定のための不事実標準回路はリング発振器である。それは、丸いチェーンにおいて接続されたインバーターの奇数から成る（図3.11）。逆転の奇数のため、この回路は操作して安定していて一理なく、発振する。

https://www.excite.co.jp/world/english/

EX_113-2 p118 [STE-101-309 line 22~ P119[STE-101-310 line 5]

通読して和文または英文で要旨をまとめてください

The period T of the oscillation is determined by the propagation time of a signal transition through the complete chain, or T = 2 x tp x N with N the number of inverters in the chain. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition. Note that this equation is only valid for 2Ntp >> tf + tr If this condition is not met, the circuit might not oscillate—one "wave" of signals propagating through the ring will overlap with a successor and eventually dampen the oscillation. Typically, a ring oscillator needs a least five stages to be operational.

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p118 [STE-101-309 line 22~ P119[STE-101-310 line 5]

STE-101-310

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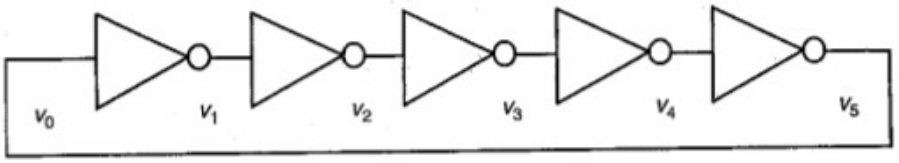
阻止する



f （周波数） = 1／T （周期）

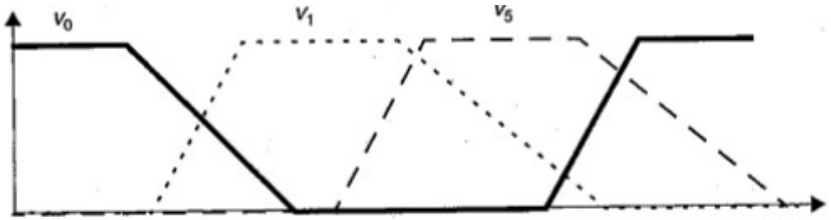


Figure 3.11 Ring oscillator circuit for propagation-delay measurement.

EX_113-2 p118 [STE-101-309 line 22~ P119[STE-101-310 line 5]自動翻訳

振動の期間Tは、Nによって完全なチェーンを通るシグナルの変遷の伝播時間、またはT = 2 X tp X Nによって決定されるチェーンのインバーターの数 。

ファクター2は、完全なサイクルが低にの高さおよび高にで低い変遷必要とする観察に起因している。

もしこの条件が満たされず、リングに伝わっているシグナルの回路不発振1の「波」が後継者と重なり、結局、振動を湿らすならば、2Ntp >> tf+tr.のためにこの方程式が有効であることにだけ注意しなさい。

一般に、稼動可能であるように、リング発振器には最もわずかな5の段階が必要である。

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通読して和文または英文で要旨をまとめてください

We must be extremely careful with results obtained from ring oscillator measurements. A tp of 100 psec by no means implies that a circuit built with those gates will operate at 10 GHz. The oscillator results are primarily useful for quantifying the differences between various manufacturing technologies and gate topologies. The oscillator is an idealized circuit where each gate has a fan-in and fan-out of exactly one and parasitic loads are minimal. In more realistic digital circuits, fan-ins and fan-outs are higher, and interconnect delays are non-negligible. The gate functionality is also substantially more complex than a simple invert operation. As a result, the achievable clock frequency on average is 50 to a 100 times slower than the frequency predicted from ring oscillator measurements. This is an average observation; carefully optimized designs might approach the ideal frequency more closely.

Example 3.3 Propagation Delay of First-Order RC Network

Digital circuits are often modeled as first-order RC networks of the type shown in Figure 3.12. The propagation delay of such a network is thus of considerable interest.

EX_113-3 p118 [STE-101-310] line 7 ~17

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私達は、リング発振器寸法から得られた結果に極めて注意しなければならない。100ピコセカンドのtpは、決して、第一に発振器結果が、様々な製造テクノロジーとゲートトポロジーの違いを定量化するのに有益な10 GHz.で、それらのゲートで組み立てられた回路が動作するのを暗示していない。発振器は、個々のゲートがファンインを持ち、ちょうど1のファンアウトおよび寄生的なロードが最小の理想化される回路である。よりリアルなデジタルの回路で、ファンインとファンアウトがより高く、遅延を相互接続する 取るに足りなくない。ゲート機能は、より複雑に大幅に1つの結果あたり1回の簡単な逆転 operation.Asよりでもあり、平均の達成可能なクロック周波数は、リング発振器寸法から予測された頻度より100倍遅さに50である。これは平均的な観察である；慎重に最適化されたデザインは、理想的な頻度により密接に近づくことができる。

Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

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