# Science and Technology English I

# Exercise 110 Meiji University 2021

(DICS Chapter-2 , MOS FET / CMOS)

EX_110_21.pptx 16 Slides June 14th.,2021

http://mikami.a.la9.jp/mdc/mdc1.htm

Renji Mikami

Renji_Mikami(at_mark)nifty.com [mikami(at_mark)meiji.ac.jp]


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# Day109 Review 1

- トランジスタとFET の構成と動作
- 制御の方法と増幅
  - トランジスタ 電流-電流制御
  - FET 電圧-電流制御
- デプレッション(P型)とエンハンス(N型)
- NとPを組み合わせるとComplementary回路
  - トランジスタ/FET (FETの場合CMOSという)
- CMOS回路が多用される理由 -> Day 110


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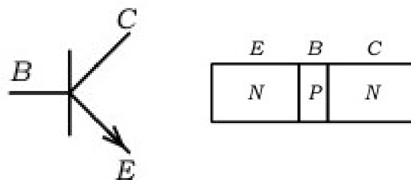
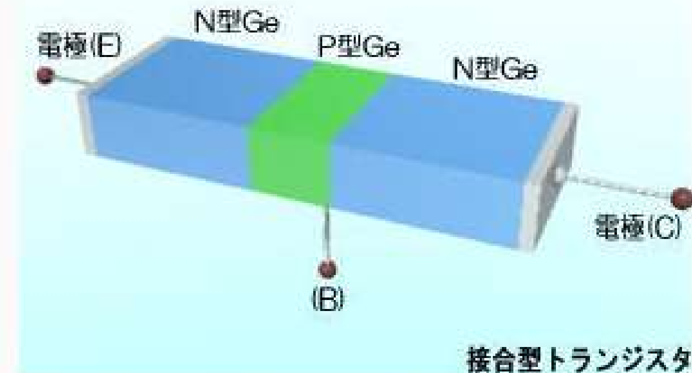
# 技術解説トランジスタ

- 2つの極 - > Diode
- **3つの極 - > Triode**：
  - トランジスタでは、ベース電流 $I_B$(ベース-エミッタ間電流)で $I_C$ コレクタ電流(コレクタ-エミッタ間電流)が変化する。この比が hFE (直流電流増幅率)




図のように、金属針(E)にプラスの電圧を、金属針(C)にマイナスの電圧をかけたとき、電極(B)の電圧次第で、E(emitter)とC(collector)の間に電流が流れたり流れなかったりすることが分かったのだ。これこそ、現在「**バイポーラトランジスタ**」と呼ばれているものの原型だった。今では、このトランジスタを「**点接触型トランジスタ**」と呼んでいる。この理論の確立にはバーディーンが大きく貢献した。

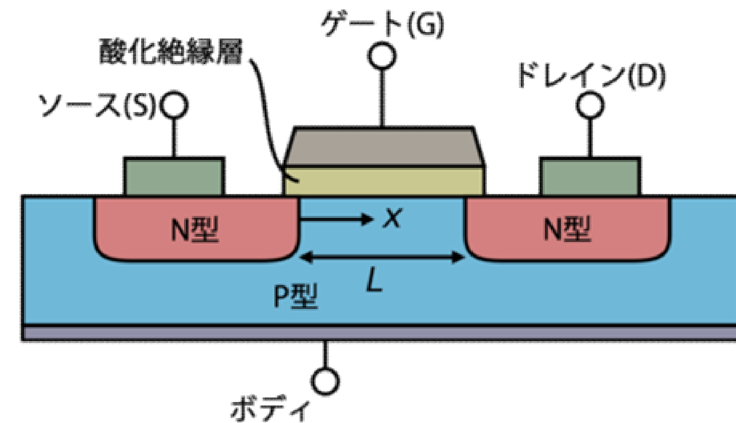
この発見を聞いたショックレーは、動作が不安定だった点接触型トランジスタを改善して、「**接合型トランジスタ**」を考案している。ちなみにトランジスタというのはベル研によって作られた名前だが、もともとは"transfer+resistor（電気を伝える抵抗素子）"という言葉からきている。




この三人は56年にトランジスタの発明・開発の業績を評価され、ノーベル物理学賞を受賞している。

# 技術解説 MOS FET /CMOS

- ゲート･ソース間電圧 $V_{GS}$ を変化させるとドレイン電流 $I_D$ が変化する。
- N チャンネルタイプは、$V_{GS}$が高くなると$I_D$が増加する(エンハンスメント型)
- P チャンネルタイプは、$V_{GS}$が高くなるとが$I_D$減少する(デプレッション型)
- N 型とP 型を組み合わせた回路がCMOS(Complementary MOS)




図版引用:ウィキペディア
https://ja.wikipedia.org/wiki/MOSFET

トランジスタ 回路との比較
トランジスタでは、$I_B$ ベース電流(ベース･エミッタ電流)で$I_C$ コレクタ電流(コレクタ-エミッタ)が変化する。この比がhFE 直流電流増幅率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# FET Spec Sheet 1

**TOSHIBA** 2SK2847

TOSHIBA FIELD EFFECT TRANSISTOR SILICON N CHANNEL MOS TYPE ($\pi$-MOSIII)

## 2SK2847

HIGH SPEED, HIGH CURRENT SWITCHING APPLICATIONS

DC-DC CONVERTER AND MOTOR DRIVE APPLICATIONS

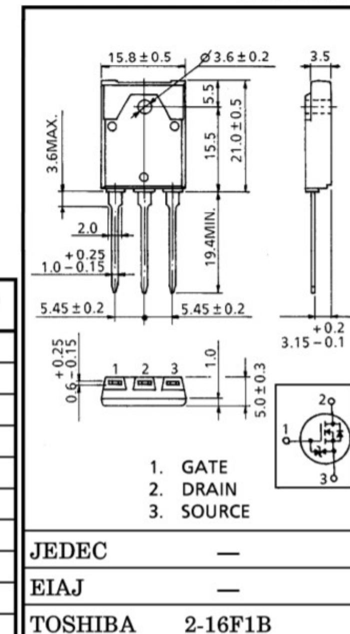
INDUSTRIAL APPLICATIONS

Unit in mm

- Low Drain-Source ON Resistance : $R_{DS\,(ON)}=1.1\Omega$ (Typ.)
- High Forward Transfer Admittance : $|Y_{fs}|=7.0S$ (Typ.)
- Low Leakage Current : $I_{DSS}=100\mu A$ (Max.) ($V_{DS}=720V$)
- Enhancement-Mode : $V_{th}=2.0\sim4.0V$ ($V_{DS}=10V$, $I_D=1mA$)

MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 900 | V |
| Drain-Gate Voltage ($R_{GS}=20k\Omega$) | | $V_{DGR}$ | 900 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±30 | V |
| Drain Current | DC | $I_D$ | 8 | A |
| | Pulse | $I_{DP}$ | 24 | A |
| Drain Power Dissipation (Tc = 25°C) | | $P_D$ | 85 | W |
| Single Pulse Avalanche Energy** | | $E_{AS}$ | 799 | mJ |
| Avalanche Current | | $I_{AR}$ | 8 | A |
| Repetitive Avalanche Energy* | | $E_{AR}$ | 8.5 | mJ |
| Channel Temperature | | $T_{ch}$ | 150 | °C |
| Storage Temperature Range | | $T_{stg}$ | −55~150 | °C |




| | |
|---|---|
| JEDEC | — |
| EIAJ | — |
| TOSHIBA | 2-16F1B |

Weight : 5.8g (Typ.)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# EX_109-32

- Do you think can we make CMOS circuit by (bipolar) transistors?
- トランジスタでもComplimentary (相補的)回路を組むことができます。1970年代には、たくさんのディスクリートのペアトランジスタ(N-cH/P-ch)が作られオーディオアンプによく使われました。
- コンプリメンタリ回路は、高性能(線形性が高い-歪みが少ない)な増幅器を実現できます。
- その後IC化が進み、ワンチップ化され近年では、アンプは(線形増幅器からPWM化-積分近似され)デジタル化(小型高能率ですが、雑音や歪みは多くなります)されています。


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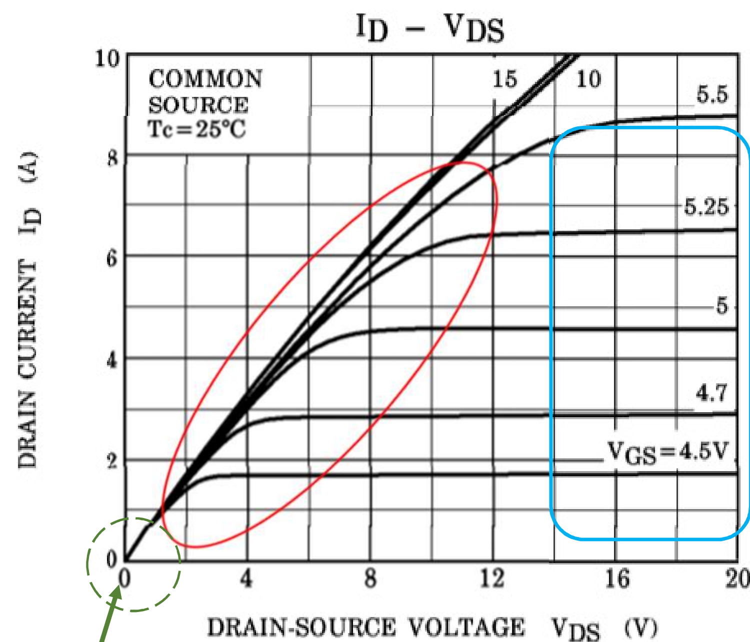
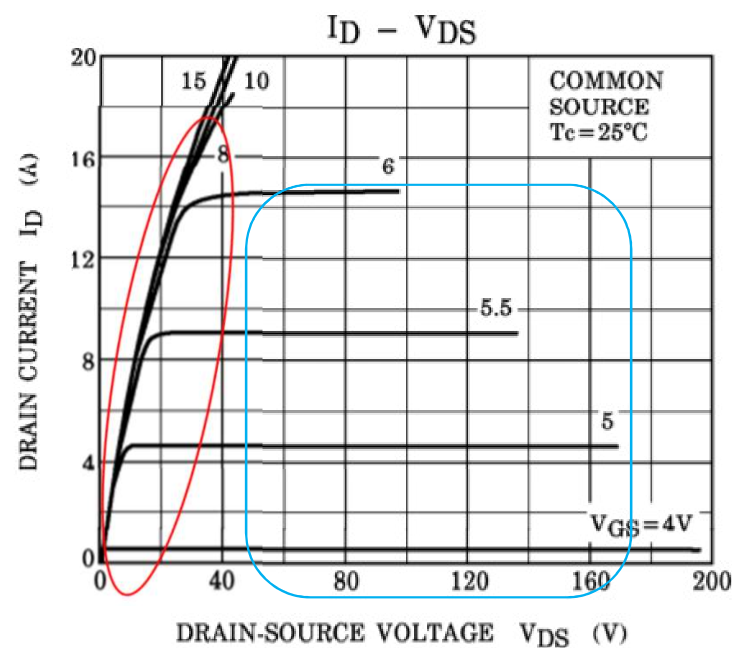
# FET Spec Sheet 2

線形領域 (triode region ) ドレイン電圧とともにドレイン電流が増える

TOSHIBA 定電流領域 ドレイン電圧が上がっても電流が一定 2SK2847




Enlarge Here - Next Slide

Triode -> 三極管特性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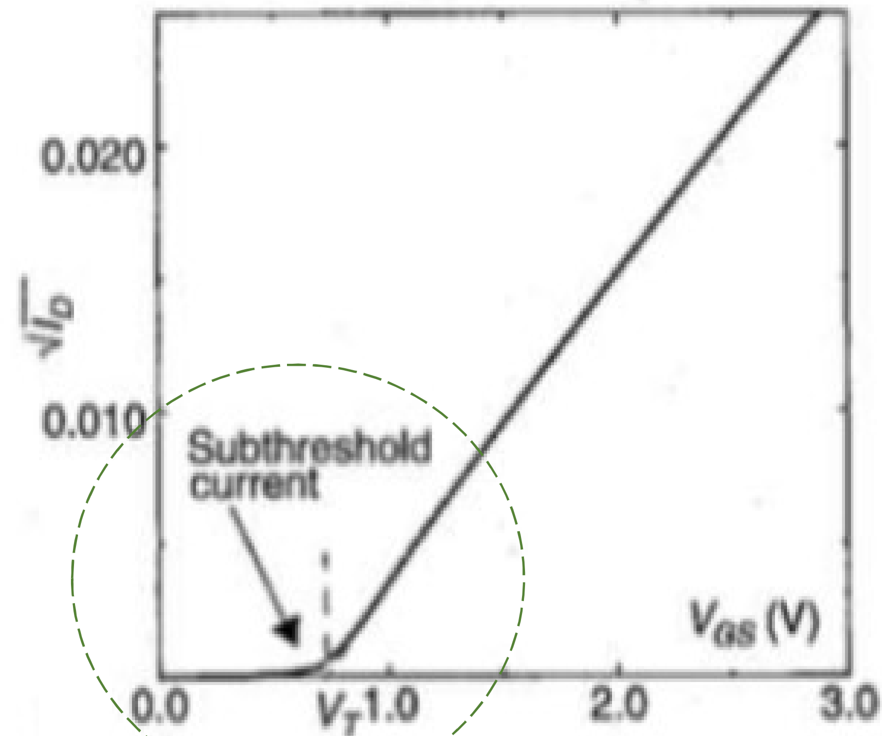
# subthreshold

ドレイン電流が遮断さ
れた状態から
流れ始めるポイント




(b) $\sqrt{I_D}$ as a function of VGS (for $V_{DS}$ = 5 V).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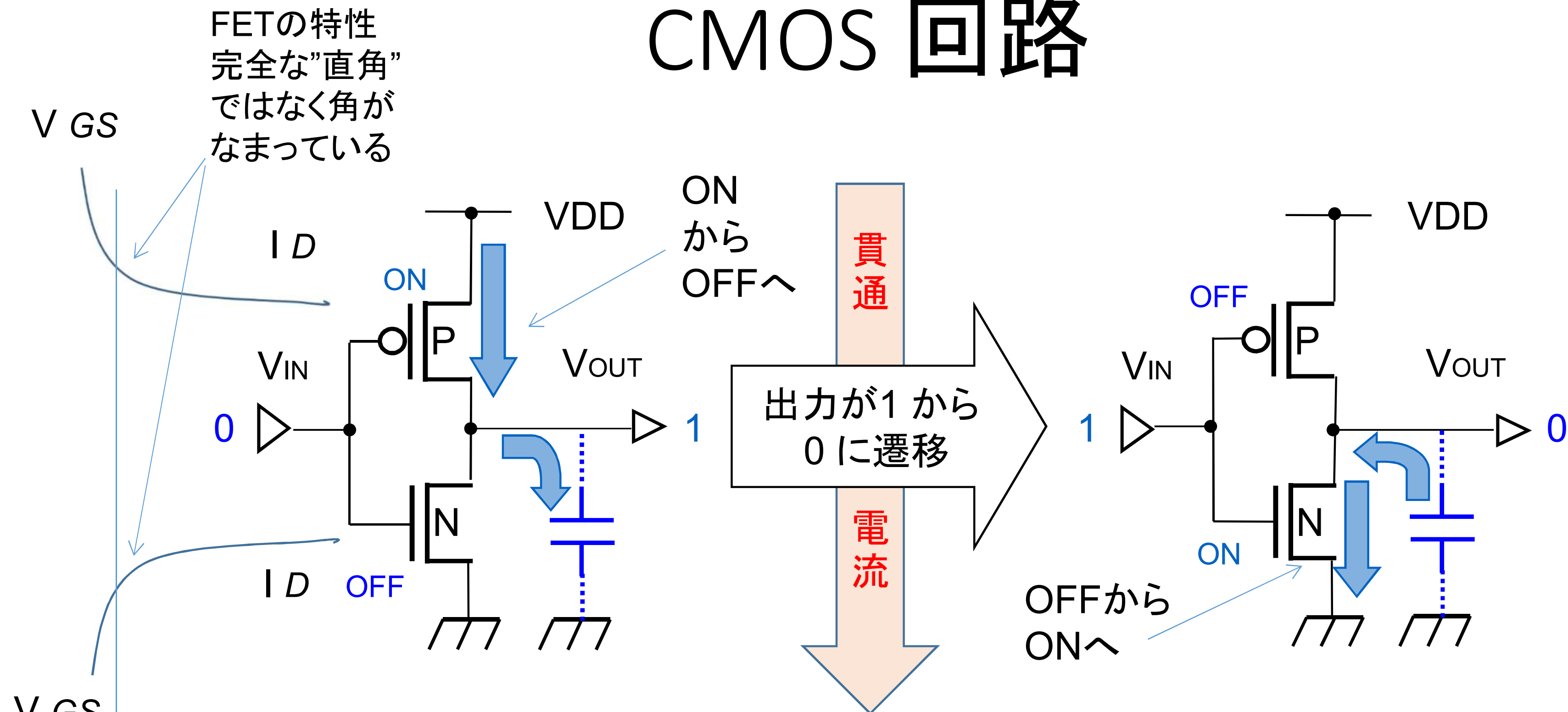
# CMOS 回路




理想動作では、上下のFETは片側はOFFだが、
実際は、双方がONとなり過渡的に電流が流れる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# Exercise: EX_110-1 p46 [STE-101-213]]

- ねらい：MOSFET の基本動作を読み取る
- *V*は電圧、*I* は電流、下付け添字 *D ドレイン, S ソース, G ゲート*
- (2.51) 11ライン(2 パラグラフ)

Execise1

Answer following questions simply (long if you like ☺).

- EX_110-11 What stands for $V_{DS}$ and $I_D$?
- EX_110-12 What is the (electric) relation between $V_{DS}$ and $I_D$?
- 提出はClass Web “レポート” にて木曜まで
- 毎回のレポートは、最低A4 1ページ以上は書いてください。余白には、今回の授業の内容、資料についての感想や要望を記入してください。


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# EX_110-1 p46 [STE-101-213]

- Figure 2.21 plots $I_D$ versus $V_{DS}$ (with $V_{GS}$ as a parameter) for an NMOS transistor. In the triode region, the transistor behaves like a voltage-controlled resistor, while in the saturation region, it acts as a voltage-controlled current source (when the channel-length modulation effect is ignored). Also shown is a plot of $I_D$ as a function of $V_{GS}$ (with $V_{DS}$ a constant). As expected a linear relationship is observed for values of $V_{GS} >> V_T$ Notice also how the current does not drop abruptly to 0 at $V_{GS} = V_T$. At that point, the device goes into subthreshold operation. To turn the device completely off, the gate-source voltage has to be substantially lower than $V_T$. Subthreshold conduction is discussed in more detail later in the chapter, when we discuss some second-order effects in MOS transistors.
- All the derived equations hold for the PMOS transistor as well. The only difference is that for PMOS devices, the polarities of all voltages and currents are reversed.


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EX_110-1 p46

[STE-101-213]

EX_110_21



電流源

~~with λ an empirical constant parameter, called the *channel-length modulation*.[3]~~

Figure 2.21 plots $I_D$ versus $V_{DS}$ (with $V_{GS}$ as a parameter) for an NMOS transistor. In the triode region, the transistor behaves like a voltage-controlled resistor, while in the saturation region, it acts as a voltage-controlled current source (when the channel-length modulation effect is ignored). Also shown is a plot of $\sqrt{I_D}$ as a function of $V_{GS}$ (with $V_{DS}$ a constant). As expected a linear relationship is observed for values of $V_{GS} >> V_T$. Notice also how the current does not drop abruptly to 0 at $V_{GS} = V_T$. At that point, the device goes into *subthreshold operation*. To turn the device completely off, the gate-source voltage has to be substantially lower than $V_T$. Subthreshold conduction is discussed in more detail later in the chapter, when we discuss some second-order effects in MOS transistors.

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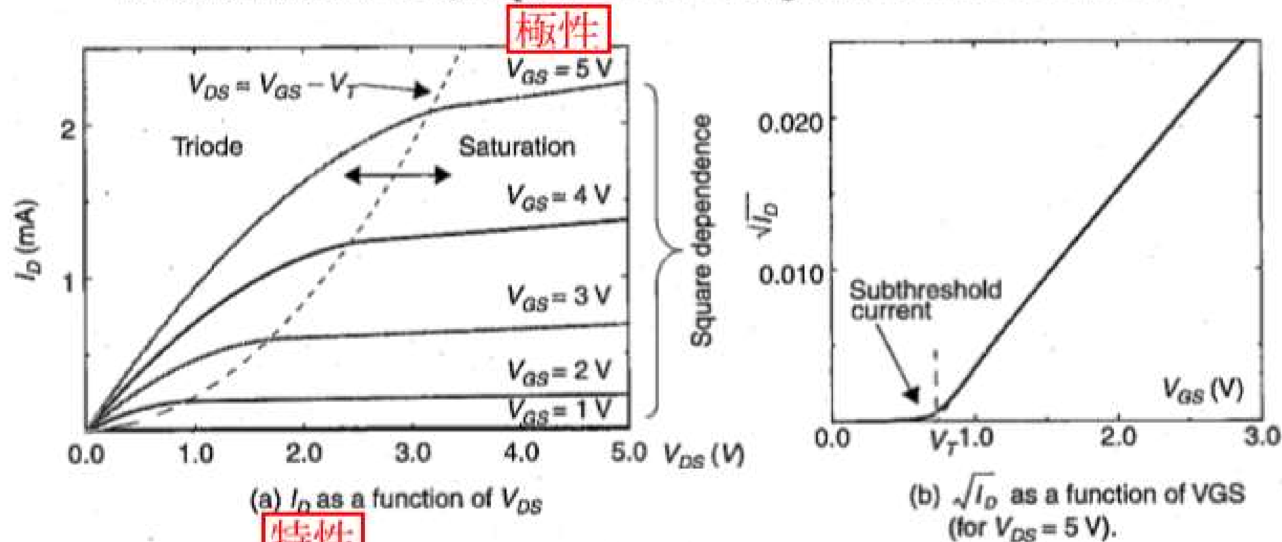


**Figure 2.21** *I-V* characteristics of NMOS transistor ($W$ = 100 μm, $L$ = 20 μm in a 1.2 μm CMOS technology).



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EX_110_21

# Exercise: EX_110-2 p47 [STE-101-214]

- ねらい：MOSFET の特性を構造面から読み取る
- 事前にネットで検索してMOSFETの基礎を調べておくこと
- 2.3.3 Dynamic Behavior もできたら読んでおく
- ターゲット文は MOS Structure Capacitors １６ライン

Figure 2.15

## Exercise

Answer following questions simply (long if you like ☺).

- EX_110-21 Why is the capacitance issue for MOS (FET) beside the (bipolar) transistor?
- EX_110-22 What type of capacitances does MOS have?
- EX_110-23 Is capacitance between Gate and Source variable?
- 提出はClass Web "レポート" にて木曜まで
- 毎回のレポートは、最低A4 1ページ以上は書いてください。余白には、今回の授業の内容、資料についての感想や要望を記入してください。

# EX_110-2 p47 [STE-101-214]

- MOS Structure Capacitances
- The gate of the MOS transistor is isolated from the conducting channel by the gate oxide that has a capacitance per unit area equal to $C_{ox} = \varepsilon_{ox}/t_{ox}$. From the I-V equations, we learned that it is useful to have Cox as large as possible, or to keep the oxide thickness very thin. The total value of this capacitance is called the gate capacitance *Cg* and equals *CoxWL*. This gate capacitance can be decomposed into a number of elements, each with a different behavior. Obviously, one part of *Cg* contributes to the channel charge, and is discussed in a subsequent section. Another part is solely due to the topological structure of the transistor. This component is the subject of the remainder of this section.
- Consider the transistor structure of Figure 2.23. Ideally, the source and drain diffusion should end right at the edge of the gate oxide. In reality, both source and drain tend to extend somewhat below the oxide by an amount xd, called the *lateral diffusion*. Hence, the effective channel of the transistor $L_{eff}$ becomes shorter than the drawn length (or the length the transistor was originally designed for) by a factor of $2x_d$. It also gives rise to a parasitic capacitance between gate and source (drain) that is called the overlap capacitance. This capacitance is strictly linear and has a fixed value

Figure 2.23


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# EX_110-2 p47 [STE-101-214]

構造 成分

## MOS Structure Capacitances

分解する 導電チャネル 横方向拡散

The gate of the MOS transistor is isolated from the conducting channel by the gate oxide that has a capacitance per unit area equal to $C_{ox} = \varepsilon_{ox} / t_{ox}$. From the *I-V* equations, we learned that it is useful to have $C_{ox}$ as large as possible, or to keep the oxide thickness very thin. The total value of this capacitance is called the *gate capacitance* $C_g$ and equals $C_{ox}WL$. This gate capacitance can be decomposed into a number of elements, each with a different behavior. Obviously, one part of $C_g$ contributes to the channel charge, and is discussed in a subsequent section. Another part is solely due to the topological structure of the transistor. This component is the subject of the remainder of this section.

位相幾何学

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寄生 重ね合わせ

Figure 2.23


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# Memo

予習：次回の資料に必ず目を通しておいてください。

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

担当講師

三上廉司(みかみれんじ)

Renji_Mikami(at_mark)nifty.com

mikami(at_mark)meiji.ac.jp (Alternative)

http://mikami.a.la9.jp/_edu.htm

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