# Science and Technology English I

# Exercise 110 Meiji University 2020

## (DICS Chapter-2 , MOS FET / CMOS)

## EX_110.pptx 10 Slides November 24th.,2019

http://mikami.a.la9.jp/mdc/mdc1.htm


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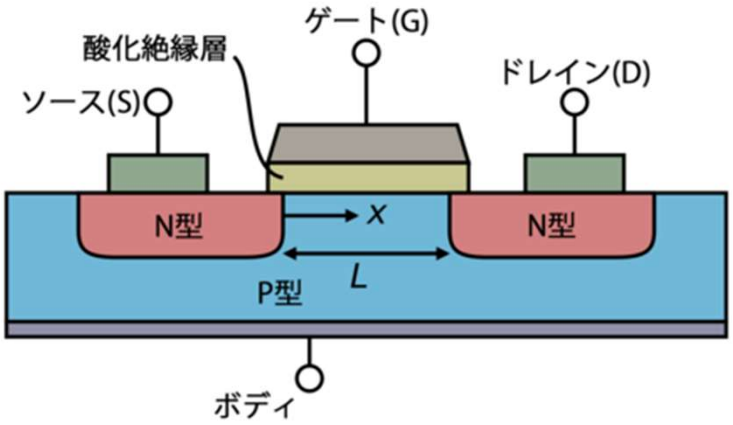
# 技術解説 MOS FET /CMOS

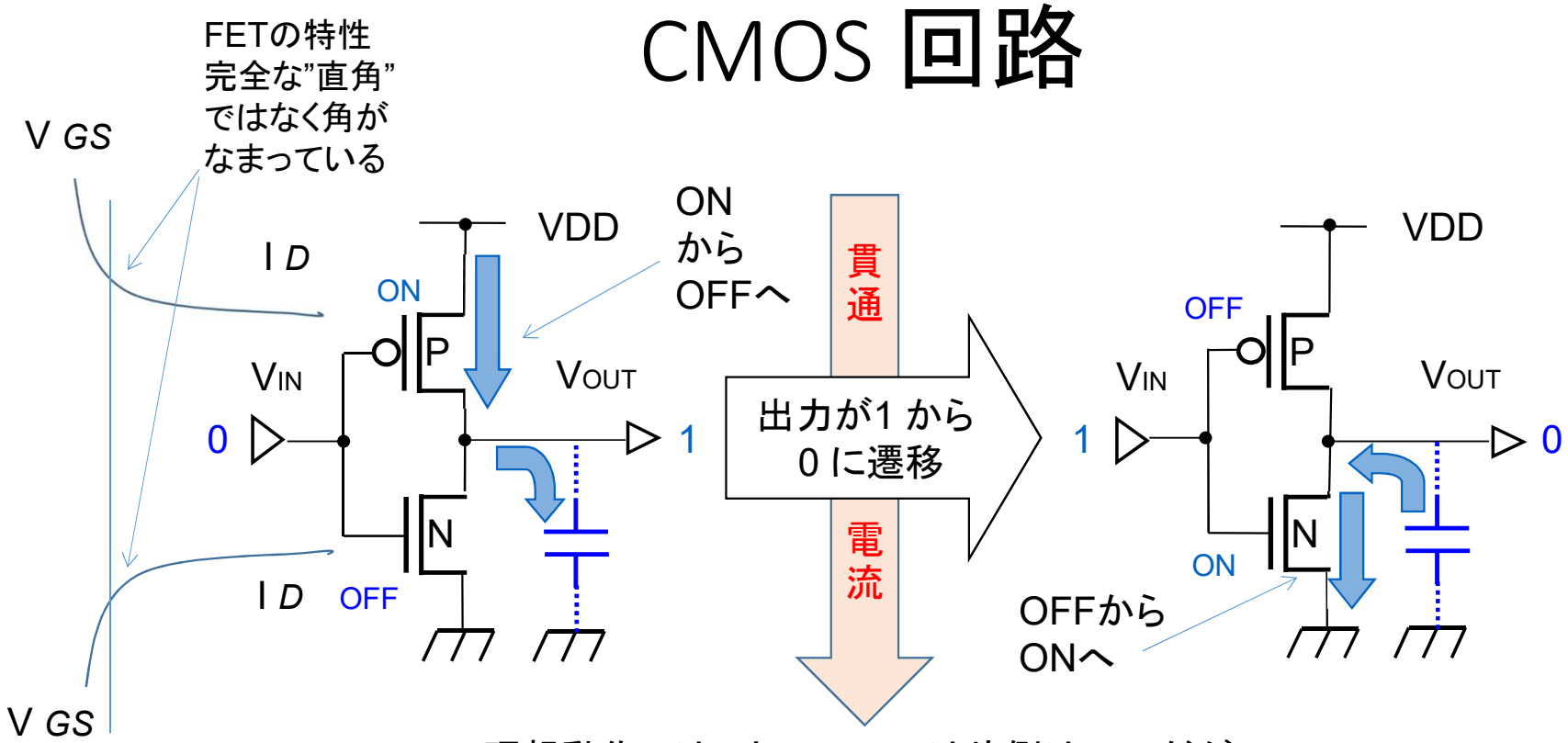
- ゲート･ソース間電圧 $V_{GS}$ を変化させるとドレイン電流 $I_D$ が変化する。
- N チャンネルタイプは、$V_{GS}$が高くなると$I_D$が増加する(エンハンスメント型)
- P チャンネルタイプは、$V_{GS}$が高くなるとが$I_D$減少する(デプレッション型)
- N 型と P 型を組み合わせた回路が CMOS(Complementary MOS)




図版引用:ウィキペディア
https://ja.wikipedia.org/wiki/MOSFET

トランジスタ 回路との比較
トランジスタでは、$I_B$ ベース電流(ベース･エミッタ電流)で$I_C$ コレクタ電流(コレクタ-エミッタ)が変化する。この比が$h_{FE}$ 直流電流増幅率

# CMOS 回路




理想動作では、上下のFETは片側はOFFだが、
実際は、双方がONとなり過渡的に電流が流れる

# Exercise: EX_110-1  p46 [STE-101-213]]

- **ねらい**: MOSFET **の基本動作を読み取る**
- *V***は電圧、***I* **は電流、下付け添字** *D ドレイン, S ソース, G ゲート*
- (2.51) **11ライン(2 パラグラフ)**

Execise1

Answer following questions simply (long if you like ☺).

- EX_110-11 What stands for $V_{DS}$ and $I_D$?
- EX_110-12 What is the (electric) relation between $V_{DS}$ and $I_D$?
- Due date : Wednesday

# EX_110-1 p46 [STE-101-213]

- Figure 2.21 plots ID versus VDS (with VGS as a parameter) for an NMOS transistor. In the triode region, the transistor behaves like a voltage-controlled resistor, while in the saturation region, it acts as a voltage-controlled current source (when the channel-length modulation effect is ignored). Also shown is a plot of ID as a function of VGS (with VDS a constant). As expected a linear relationship is observed for values of VGS >> VT Notice also how the current does not drop abruptly to 0 at VGS = VT. At that point, the device goes into subthreshold operation. To turn the device completely off, the gate-source voltage has to be substantially lower than VT Subthreshold conduction is discussed in more detail later in the chapter, when we discuss some second-order effects in MOS transistors.
- All the derived equations hold for the PMOS transistor as well. The only difference is that for PMOS devices, the polarities of all voltages and currents are reversed.

EX_110-1 p46

[STE-101-213]



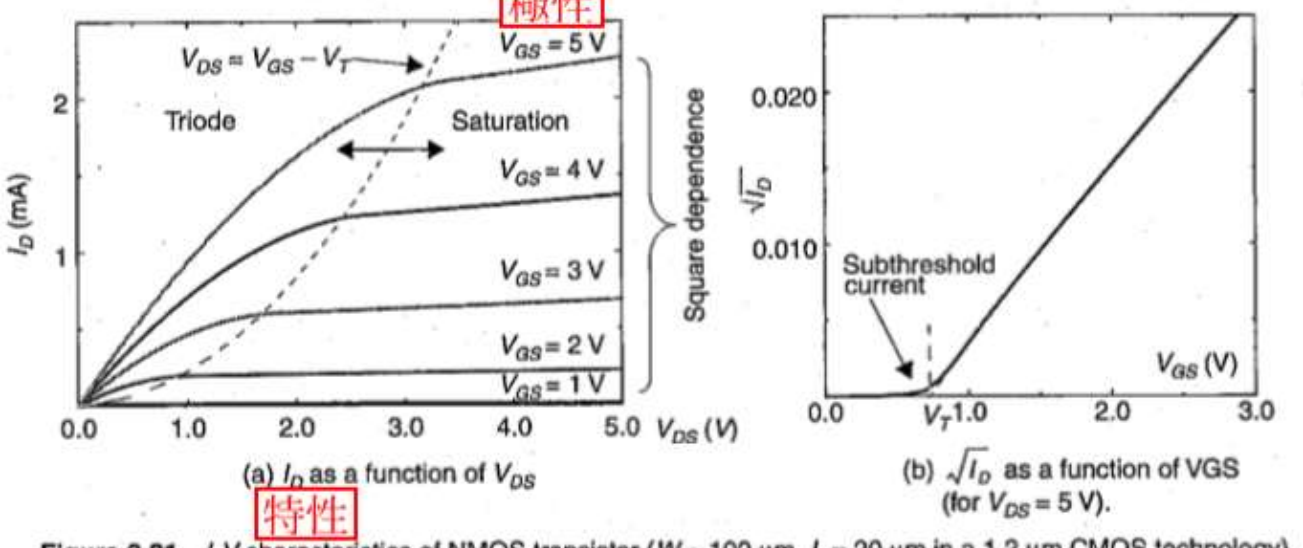
電流源

~~with λ an empirical constant parameter, called the *channel-length modulation*.~~[3]

Figure 2.21 plots $I_D$ versus $V_{DS}$ (with $V_{GS}$ as a parameter) for an NMOS transistor. In the triode region, the transistor behaves like a voltage-controlled resistor, while in the saturation region, it acts as a voltage-controlled current source (when the channel-length modulation effect is ignored). Also shown is a plot of $\sqrt{I_D}$ as a function of $V_{GS}$ (with $V_{DS}$ a constant). As expected a linear relationship is observed for values of $V_{GS} >> V_T$. Notice also how the current does not drop abruptly to 0 at $V_{GS} = V_T$. At that point, the device goes into *subthreshold operation*. To turn the device completely off, the gate-source voltage has to be substantially lower than $V_T$. Subthreshold conduction is discussed in more detail later in the chapter, when we discuss some second-order effects in MOS transistors.

All the derived equations hold for the PMOS transistor as well. The only difference is that for PMOS devices, the polarities of all voltages and currents are reversed.

極性




(a) $I_D$ as a function of $V_{DS}$

(b) $\sqrt{I_D}$ as a function of VGS (for $V_{DS} = 5$ V).

特性

**Figure 2.21** *I-V* characteristics of NMOS transistor ($W = 100$ µm, $L = 20$ µm in a 1.2 µm CMOS technology).

# Exercise: EX_110-2 p47 [STE-101-214]

- ねらい: MOSFET の特性を構造面から読み取る
- 事前にネットで検索してMOSFETの基礎を調べておくこと
- 2.3.3 Dynamic Behavior もできたら読んでおく
- ターゲット文は MOS Structure Capacitors １６ライン

Figure 2.15

## Exercise

Answer following questions simply (long if you like ☺).

- EX_110-21 Why is the capacitance issue for MOS (FET) beside the (bipolar) transistor?
- EX_110-22 What type of capacitances does MOS have?
- EX_110-23 Is capacitance between Gate and Source variable?
- Due date : Wednesday

# EX_110-2 p47 [STE-101-214]

- MOS Structure Capacitances
- The gate of the MOS transistor is isolated from the conducting channel by the gate oxide that has a capacitance per unit area equal to Cox = εox/tox. From the I-V equations, we learned that it is useful to have Cox as large as possible, or to keep the oxide thickness very thin. The total value of this capacitance is called the gate capacitance Cg and equals CoxWL. This gate capacitance can be decomposed into a number of elements, each with a different behavior. Obviously, one part of Cg contributes to the channel charge, and is discussed in a subsequent section. Another part is solely due to the topological structure of the transistor. This component is the subject of the remainder of this section.
- Consider the transistor structure of Figure 2.23. Ideally, the source and drain diffusion should end right at the edge of the gate oxide. In reality, both source and drain tend to extend somewhat below the oxide by an amount xd, called the lateral diffusion. Hence, the effective channel of the transistor Leff becomes shorter than the drawn length (or the length the transistor was originally designed for) by a factor of 2 xd. It also gives rise to a parasitic capacitance between gate and source (drain) that is called the overlap capacitance. This capacitance is strictly linear and has a fixed value

Figure 2.23

# EX_110-2 p47 [STE-101-214]

構造 成分

## MOS Structure Capacitances

分解する 導電チャネル 横方向拡散

The gate of the MOS transistor is isolated from the conducting channel by the gate oxide that has a capacitance per unit area equal to $C_{ox} = \varepsilon_{ox} / t_{ox}$. From the *I-V* equations, we learned that it is useful to have $C_{ox}$ as large as possible, or to keep the oxide thickness very thin. The total value of this capacitance is called the *gate capacitance* $C_g$ and equals $C_{ox}WL$. This gate capacitance can be decomposed into a number of elements, each with a different behavior. Obviously, one part of $C_g$ contributes to the channel charge, and is discussed in a subsequent section. Another part is solely due to the topological structure of the transistor. This component is the subject of the remainder of this section.

位相幾何学

Consider the transistor structure of Figure 2.23. Ideally, the source and drain diffusion should end right at the edge of the gate oxide. In reality, both source and drain tend to extend somewhat below the oxide by an amount $x_d$, called the *lateral diffusion*. Hence, the effective channel of the transistor $L_{eff}$ becomes shorter than the drawn length (or the length the transistor was originally designed for) by a factor of $2x_d$. It also gives rise to a parasitic capacitance between gate and source (drain) that is called the *overlap capacitance*. This capacitance is strictly linear and has a fixed value

寄生

重ね合わせ

Figure 2.23

# Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

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