Science and Technology English I

Exercise 109 Meiji University 2021

(DICS Chapter-2 , Transistor / MOS FET)

EX_109_21.pptx 19 Slides June14th.,2022

http://mikami.a.la9.jp/mdc/mdc1.htm

Renji Mikami

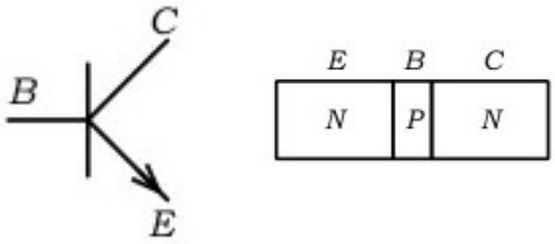
Renji_Mikami(at_mark)nifty.com [mikami(at_mark)meiji.ac.jp]

Day 109 Exercise

- FETとトランジスタのポイント解説 - この演習は最初に概容速読をして、2回目に技術内容読込に入ります。2回目は時間かけて読んでもいいです。
- 英文の質問を理解する
  - 学校英語力(正確に理解する必要がある)
- 技術英文から内容を読み取る
  - Inbound Reading のExercise
- 英文で質問に答える
  - Outbound Writing のExercise
  - 長文で答えてもよい。その場合は、起承転結、序破急で書いてみよう

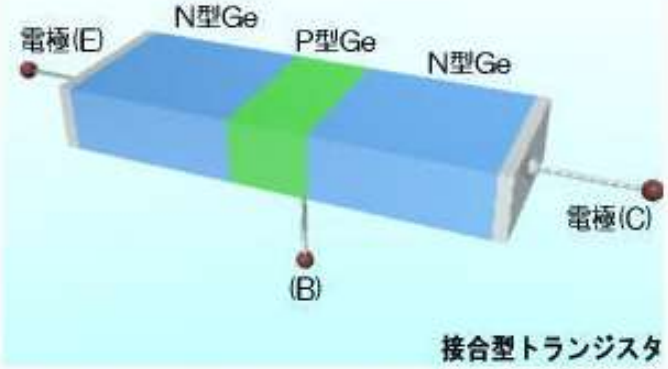
技術解説トランジスタ

- トランジスタでは、ベース電流 I_B(ベース-エミッタ間電流)で Ic コレクタ電流(コレクタ-エミッタ間電流)が変化する。この比が hFE (直流電流増幅率)



図のように、金属針(E)にプラスの電圧を、金属針(C)にマイナスの電圧をかけたとき、電極(B)の電圧次第で、E(emitter)とC(collector)の間に電流が流れたり流れなかったりすることが分かったのだ。これこそ、現在「**バイポーラトランジスタ**」と呼ばれているものの原型だった。今では、このトランジスタを「**点接触型トランジスタ**」と呼んでいる。この理論の確立にはバーディーンが大きく貢献した。

この発見を聞いたショックレーは、動作が不安定だった点接触型トランジスタを改善して、「**接合型トランジスタ**」を考案している。ちなみにトランジスタというのはベル研によって作られた名前だが、もともとは"transfer+resistor（電気を伝える抵抗素子）"という言葉からきている。



この三人は56年にトランジスタの発明・開発の業績を評価され、ノーベル物理学賞を受賞している。

EX_109_21

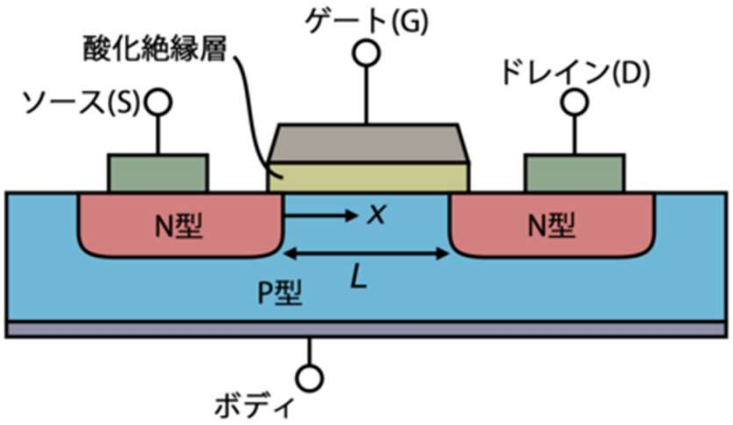
技術解説 MOS FET

ゲート･ソース間電圧 V_{GS} を変化させるとドレイン電流 I_D が変化する。

N チャンネルタイプは、V_{GS}が高くなるとI_Dが増加する(エンハンスメント型)

P チャンネルタイプは、V_{GS}が高くなるとがI_D減少する(デプレッション型)

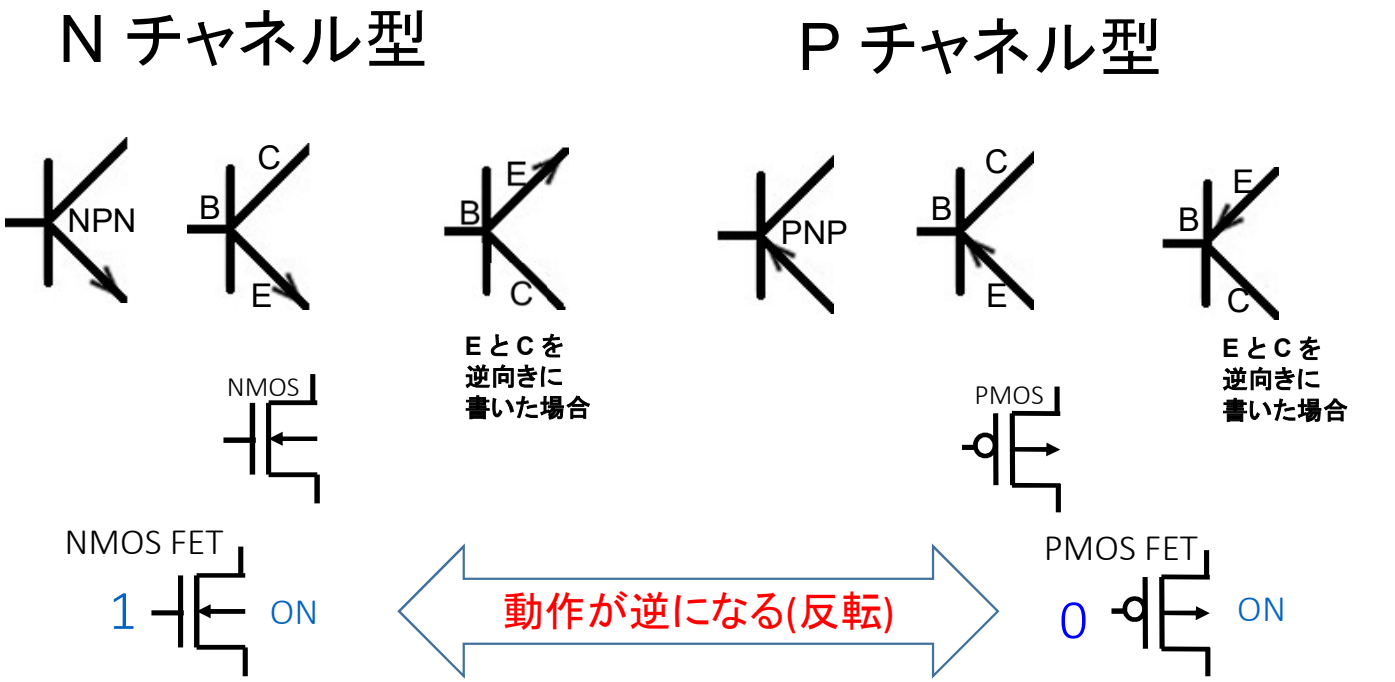
N型とP型を組み合わせた回路がCMOS(Complementary MOS)



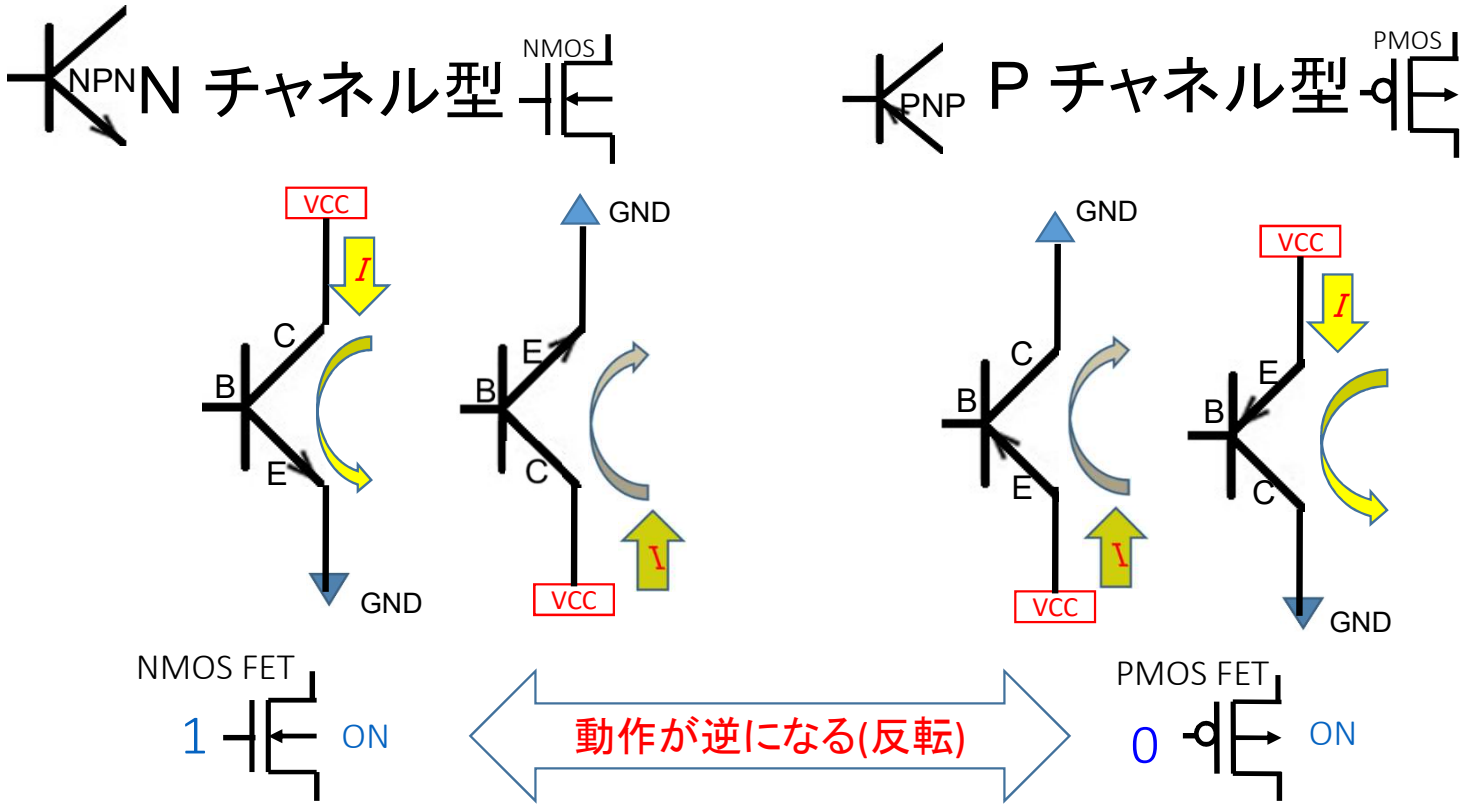
図版引用:ウィキペディア
https://ja.wikipedia.org/wiki/MOSFET

トランジスタ 回路とFETの回路の比較
トランジスタは、ベース電流でコレクタ電流がをコントロール(電流-電流制御)
FETはゲート電圧でドレイン電流をコントロールする(電圧-電流制御)

トランジスタとFETの記号



電流の流れる方向



入力側が1のとき
電流が流れる

入力側が0のとき
電流が流れる

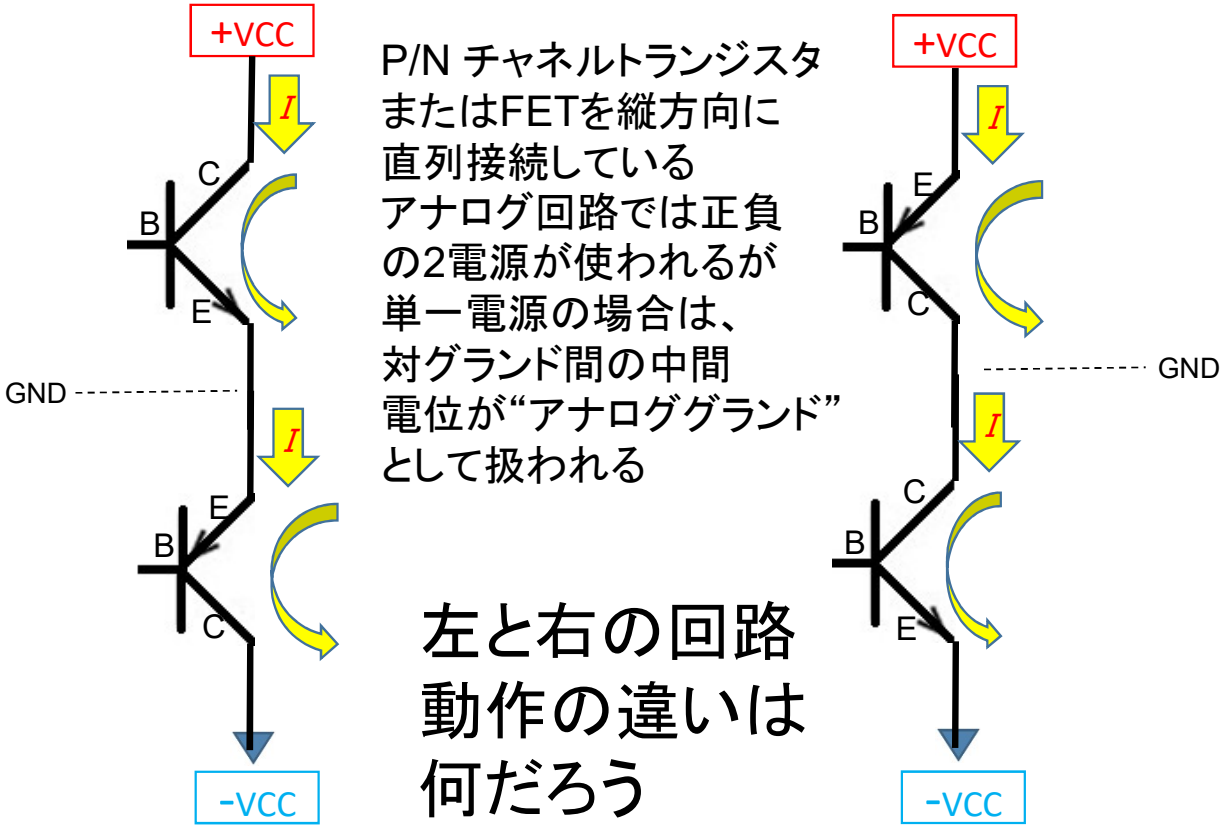
Complementary回路

- Complementary 回路はNチャネルとPチャネル半導体を縦方向に接続して、相補的(Complementary)な回路動作をさせるもの
- まず縦方向に接続して上から下に電流を流すことを考えてみる。
- この方法には2通りあることが見えればよい
- デジタルのCMOS回路では、このうちの1つがインバータとして使われる。

相補(Complementary)接続

N チャネルが+側

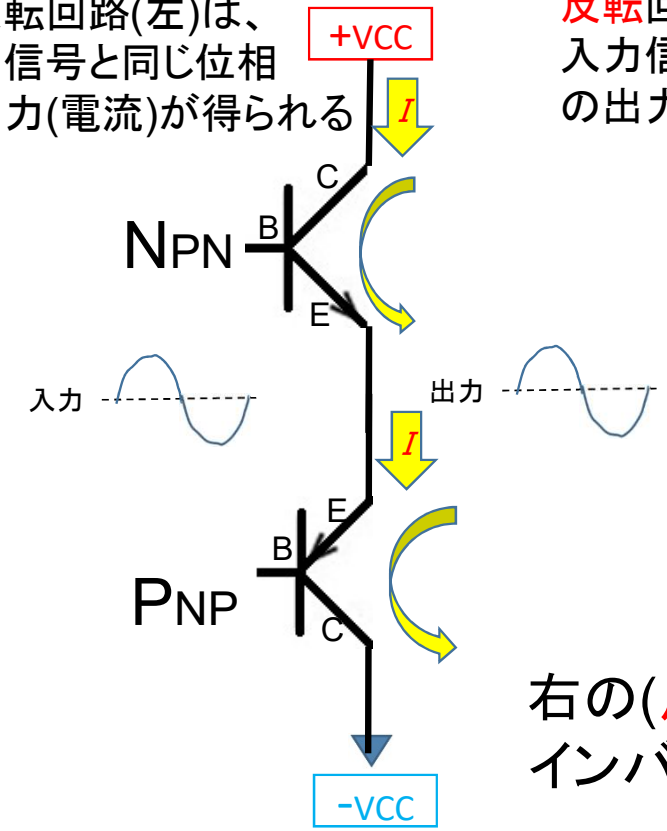
P チャネル型が+側



相補(Complementary)接続

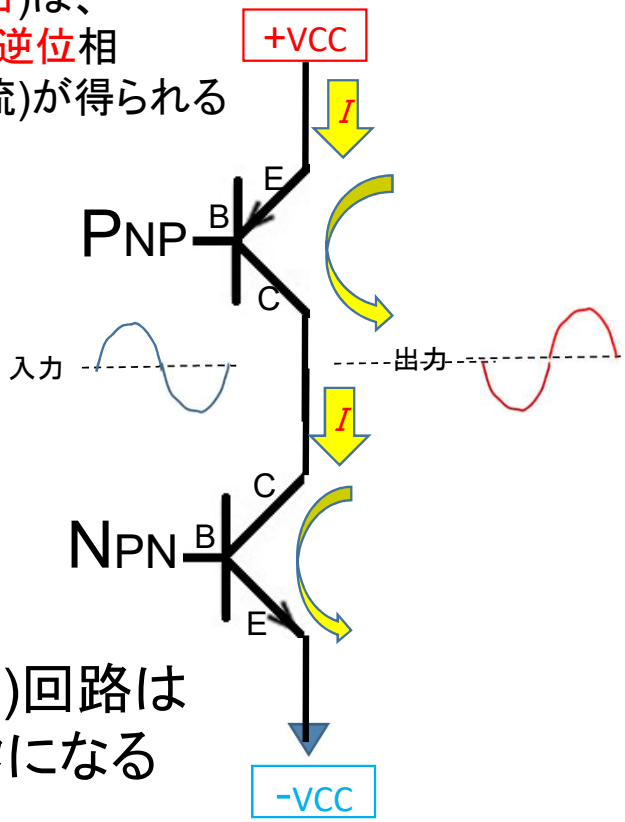
非反転回路

非反転回路(左)は、
入力信号と同じ位相
の出力(電流)が得られる



反転回路

反転回路(右)は、
入力信号と逆位相
の出力(電流)が得られる



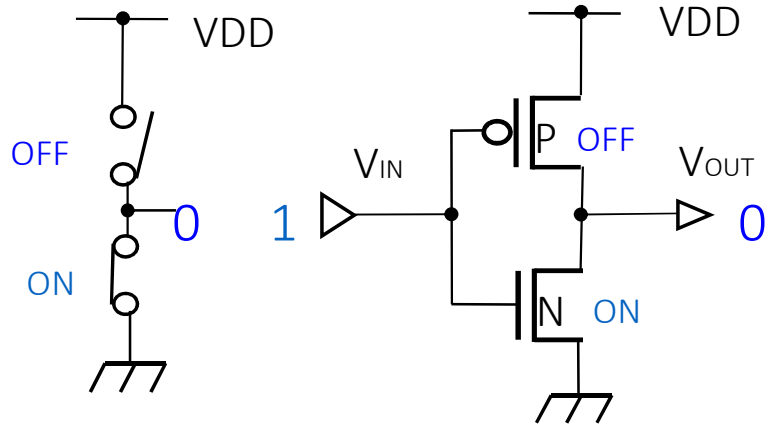
右の(反転)回路は
インバータになる

FET(CMOS) 反転回路

PMOS FET

0 ON

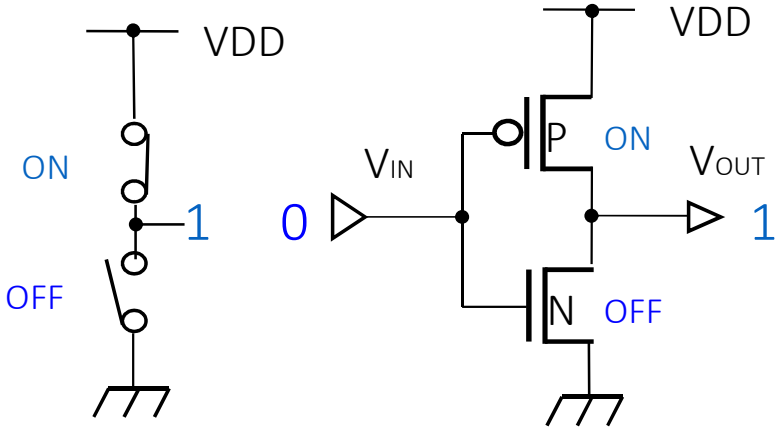
Vinが1のときは，PMOSがOFF, NMOSがON.
よってVOUTは0になる.



NMOS FET

1 ON

Vinが0のときは，PMOSがON, NMOSがOFF.
よってVOUTは1になる.



Exercise: EX_109-1 p39 [STE-101-206]

- ねらい : MOSFET の概要を読み取る
- 2.3 The MOS(FET) Transistor
- 9ライン(2 パラグラフ)

Exercise

Answer following questions simply (long if you like ☺).

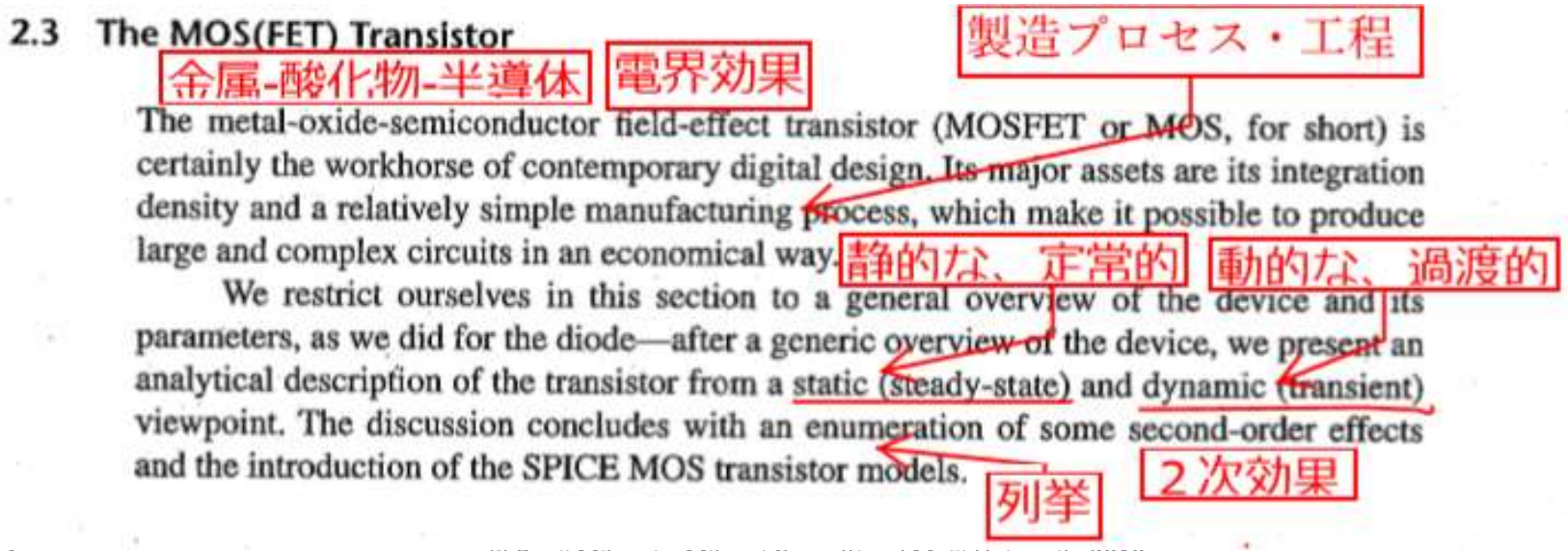
- EX_109-11 What is the major advantage of MOS FET?
- EX_109-12 We focus what in this section?
- Due date : Thursday

EX_109-1 p39 [STE-101-206]

2.3 The MOS(FET) Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET or MOS, for short) is certainly the workhorse of contemporary digital design. Its major assets are its integration density and a relatively simple manufacturing process, which make it possible to produce large and complex circuits in an economical way.

We restrict ourselves in this section to a general overview of the device and its parameters, as we did for the diode after a generic overview of the device, we present an analytical description of the transistor from a static (steady-state) and dynamic (transient) viewpoint. The discussion concludes with an enumeration of some second-order effects and the introduction of the SPICE MOS transistor models.



EX_109_21

Exercise: EX_109-2 p39 [STE-101-206]-p40[-207]

- ねらい: MOSFET の構造を技術的に読み取る
- 2.3.1 A First Glance at the Device
- 8ライン

Figure 2.15

Exercise

Answer following questions simply (long if you like ☺).

- EX_109-21 Channels are separated (insulated) by what?
- EX_109-22 What conductive material is commonly used?
- EX_109-23 What do you think about the major difference between transistor and FET?
- Due date : Thursday

EX_109-2 p39 [STE-101-206]

EX_109_21

- 2.3.1 A First Glance at the Device
- A cross section of a typical n-channel MOS transistor (NMOS) is shown in Figure 2.15. Heavily doped *n*-type source and drain regions are implanted (or diffused) into a lightly doped *p*-type substrate (often called the *body*). A thin layer of silicon dioxide (SiO_2) is grown over the region between the source and drain and is covered by a conductive material, most often polycrystalline silicon (or polysilicon, for short).
- The conductive material forms the gate of the transistor. Neighboring devices are insulated from each other with the aid of a thick layer of SiO_2 (called the field oxide) and a reverse-biased np-diode, formed by adding an extra p+ region, called the *channel-stop implant (or field implant)*.

Figure 2.15

EX_109-2 p39 [STE-101-206]

EX_109_21

2.3.1 A First Glance at the Device

断面図

注入or拡散

シリコン酸化膜

基板

A cross section of a typical *n*-channel MOS transistor (NMOS) is shown in Figure 2.15. Heavily doped *n*-type *source* and *drain* regions are implanted (or diffused) into a lightly doped *p*-type substrate (often called the *body*). A thin layer of silicon dioxide (SiO_2) is grown over the region between the source and drain and is covered by a conductive material, most often polycrystalline silicon (or polysilicon, for short). The conductive material

多結晶

導電性材料

絶縁

forms the *gate* of the transistor. Neighboring devices are insulated from each other with the aid of a thick layer of SiO_2 (called the *field oxide*) and a reverse-biased *np*-diode, formed by adding an extra p^+ region, called the *channel-stop implant* (or *field implant*).

逆バイアス電圧

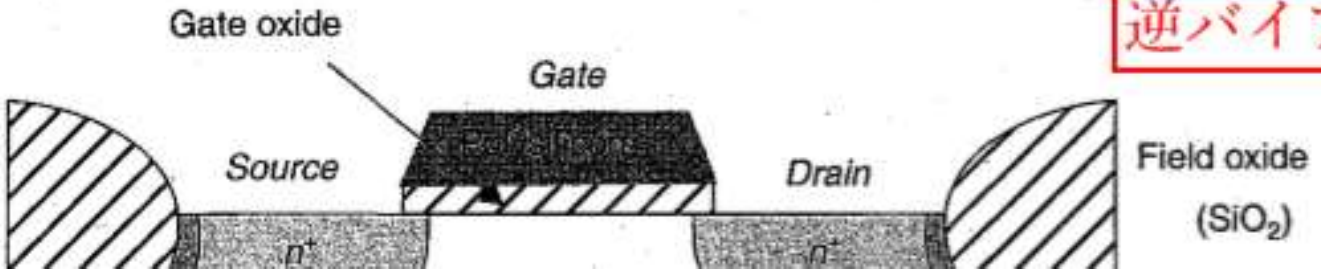


Figure 2.15

Exercise: EX_109-3 p40 [STE-101-207]

- At the most superficial level ~　から28行目まで
- Exercise

Answer following questions simply (long if you like ☺).

- EX_109-31 What stands for NMOS, PMOS and CMOS?
- EX_109-32 Do you think can we make CMOS circuit by (bipolar) transistors?
- EX_109-33 Why do you think so?

提出はClass Web “レポート” にて木曜まで
毎回のレポートは、最低A4 1ページ以上は書いてください。余白には、今回の授業の内容、資料についての感想や要望を記入してください。

EX_109-3 p40 [STE-101-207]

- At the most superficial level, the NMOS transistor can be considered to act as a switch. When a voltage is applied to the gate that is larger than a given value called the *threshold voltage* V_T a conducting channel is formed between drain and source. In the presence of a voltage difference between drain and source, current flows between the two. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the channel resistance and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.
- In an NMOS transistor, current is carried by electrons moving through an n-type channel between source and drain. This is in contrast with the *pn*-junction diode, where current is carried by both holes and electrons. MOS devices can also be made by using an *n*-type substrate and *p*+ drain and source regions. In such a transistor, current is carried by holes moving through a *p*-type channel. Such a device is called a *p*-channel MOS, or PMOS transistor. In a complementary MOS technology (CMOS), both devices are present. In a pure NMOS or PMOS technology, the substrate is common to all devices and invariably connected to dc power supply voltage. In CMOS technology, PMOS and NMOS devices are fabricated in separate isolated regions called *wells* that are connected to different power supplies. Figure 2.16 shows a cross-section of a CMOS device, where PMOS transistors are implemented in a *n*-type area embedded in a *p*-type substrate. For obvious reasons, such a fabrication approach is called an *n-well* technology.

EX_109_21

EX_109-3 p40 [STE-101-207]

Figure 2.15 Cross section of NMOS transistor.

閾値電圧

断面図

変調

At the most superficial level, the NMOS transistor can be considered to act as a switch. When a voltage is applied to the gate that is larger than a given value called the *threshold voltage* V_T, a conducting channel is formed between drain and source. In the presence of a voltage difference between drain and source, current flows between the two. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the channel resistance and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.

正孔と電子

相補的

In an NMOS transistor, current is carried by electrons moving through an *n*-type channel between source and drain. This is in contrast with the *pn*-junction diode, where current is carried by both holes and electrons. MOS devices can also be made by using an *n*-type substrate and p^+ drain and source regions. In such a transistor, current is carried by holes moving through a *p*-type channel. Such a device is called a *p*-channel MOS, or PMOS transistor. In a complementary MOS technology (CMOS), both devices are present. In a pure NMOS or PMOS technology, the substrate is common to all devices and invariably connected to dc power supply voltage. In CMOS technology, PMOS and NMOS devices are fabricated in separate isolated regions called *wells* that are connected to different power supplies. Figure 2.16 shows a cross-section of a CMOS device, where PMOS transistors are implemented in a *n*-type area embedded in a *p*-type substrate. For obvious reasons, such a fabrication approach is called an *n-well* technology.

電源

組み込み

Circuit symbols for the various MOS transistors are shown in Figure 2.17. In gen

Memo

予習：次回の資料に必ず目を通しておいてください。

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

担当講師

三上廉司(みかみれんじ)

Renji_Mikami(at_mark)nifty.com

mikami(at_mark)meiji.ac.jp (Alternative)

http://mikami.a.la9.jp/_edu.htm