

Science and Technology English I

Exercise 109 Meiji University 2020

(DICS Chapter-2 , Transistor / MOS FET)

EX_109.pptx 12 Slides November 24th, 2019

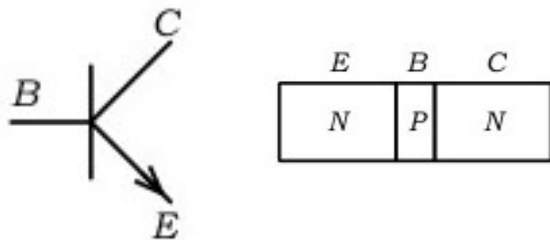
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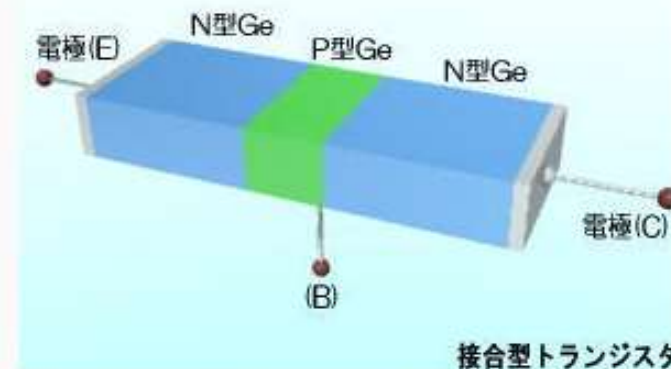
技術解説 トランジスタ

- トランジスタでは、ベース電流 I_B (ベース-エミッタ間電流) で I_C コレクタ電流(コレクタ-エミッタ間電流)が変化する。この比が hFE (直流電流増幅率)



図のように、金属針(E)にプラスの電圧を、金属針(C)にマイナスの電圧をかけたとき、電極(B)の電圧次第で、E(emitter)とC(collector)の間に電流が流れたり流れなかったりすることが分かったのだ。これこそ、現在「**バイポーラトランジスタ**」と呼ばれているものの原型だった。今では、このトランジスタを「**点接触型トランジスタ**」と呼んでいる。この理論の確立にはバーディーンが大きく貢献した。

この発見を聞いたショックレーは、動作が不安定だった点接触型トランジスタを改善して、「**接合型トランジスタ**」を考案している。ちなみにトランジスタというのはベル研によって作られた名前だが、もともとは"transfer+resistor (電気を伝える抵抗素子)"という言葉からきている。



この三人は56年にトランジスタの発明・開発の業績を評価され、ノーベル物理学賞を受賞している。

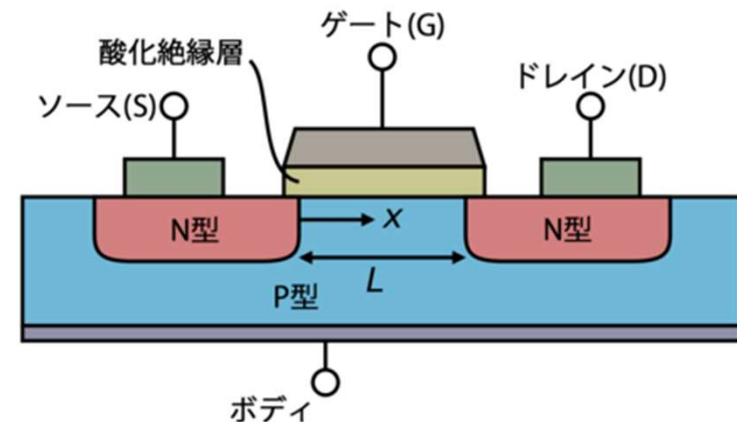
技術解説 MOS FET

ゲート・ソース間電圧 V_{GS} を変化させるとド레인電流 I_D が変化する。

N チャンネルタイプは、 V_{GS} が高くなると I_D が増加する(エンハンスメント型)

P チャンネルタイプは、 V_{GS} が高くなると I_D 減少する(デプレッション型)

N型とP型を組み合わせた回路が CMOS(Complementary MOS)



図版引用:ウィキペディア

<https://ja.wikipedia.org/wiki/MOSFET>

トランジスタ 回路とFETの回路の比較
トランジスタは、ベース電流でコレクタ電流がをコントロール(**電流-電流制御**)
FETはゲート電圧でド레인電流をコントロールする(**電圧-電流制御**)

Exercise: EX_109-1 p39 [STE-101-206]

- ねらい: MOSFET の概要を読み取る
- 2.3 The MOS(FET) Transistor
- 9ライン(2 パラグラフ)

Exercise

Answer following questions simply (long if you like 😊).

- EX_109-11 What is the major advantage of MOS FET?
- EX_109-12 We focus what in this section?
- Due date : Wednesday

EX_109-1 p39 [STE-101-206]

2.3 The MOS(FET) Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET or MOS, for short) is certainly the workhorse of contemporary digital design. Its major assets are its integration density and a relatively simple manufacturing process, which make it possible to produce large and complex circuits in an economical way.

We restrict ourselves in this section to a general overview of the device and its parameters, as we did for the diode after a generic overview of the device, we present an analytical description of the transistor from a static (steady-state) and dynamic (transient) viewpoint. The discussion concludes with an enumeration of some second-order effects and the introduction of the SPICE MOS transistor models.

2.3 The MOS(FET) Transistor

金属-酸化物-半導体 電界効果

製造プロセス・工程

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静的な、定常的 動的な、過渡的

We restrict ourselves in this section to a general overview of the device and its parameters, as we did for the diode—after a generic overview of the device, we present an analytical description of the transistor from a static (steady-state) and dynamic (transient) viewpoint. The discussion concludes with an enumeration of some second-order effects and the introduction of the SPICE MOS transistor models.

列挙

2次効果

Exercise: EX_109-2 p39 [STE-101-206]-p40[-207]

- ねらい: MOSFET の構造を技術的に読み取る
- 2.3.1 A First Glance at the Device
- 8ライン

Figure 2.15

Exercise

Answer following questions simply (long if you like 😊).

- EX_109-21 Channels are separated (insulated) by what?
- EX_109-22 What conductive material is commonly used?
- EX_109-23 What do you think about the major difference between transistor and FET?
- Due date : Wednesday

EX_109-2 p39 [STE-101-206]

- 2.3.1 A First Glance at the Device
- A cross section of a typical n-channel MOS transistor (NMOS) is shown in Figure 2.15. Heavily doped n-type source and drain regions are implanted (or diffused) into a lightly doped p-type substrate (often called the body). A thin layer of silicon dioxide (SiO_2) is grown over the region between the source and drain and is covered by a conductive material, most often polycrystalline silicon (or polysilicon, for short). The conductive material
- forms the gate of the transistor. Neighboring devices are insulated from each other with the aid of a thick layer of SiO_2 (called the field oxide) and a reverse-biased np-diode, formed by adding an extra region, called the channel-stop implant (or field implant).

Figure 2.15

2.3.1 A First Glance at the Device

断面図

注入or拡散

シリコン酸化膜

基板

A cross section of a typical *n*-channel MOS transistor (NMOS) is shown in Figure 2.15. Heavily doped *n*-type *source* and *drain* regions are implanted (or diffused) into a lightly doped *p*-type substrate (often called the *body*). A thin layer of silicon dioxide (SiO_2) is grown over the region between the source and drain and is covered by a conductive material, most often polycrystalline silicon (or polysilicon, for short). The conductive material

多結晶

導電性材料

40

絶縁

THE DEVICES Chapter 2

forms the *gate* of the transistor. Neighboring devices are insulated from each other with the aid of a thick layer of SiO_2 (called the *field oxide*) and a reverse-biased *np*-diode, formed by adding an extra p^+ region, called the *channel-stop implant* (or *field implant*).

逆バイアス電圧

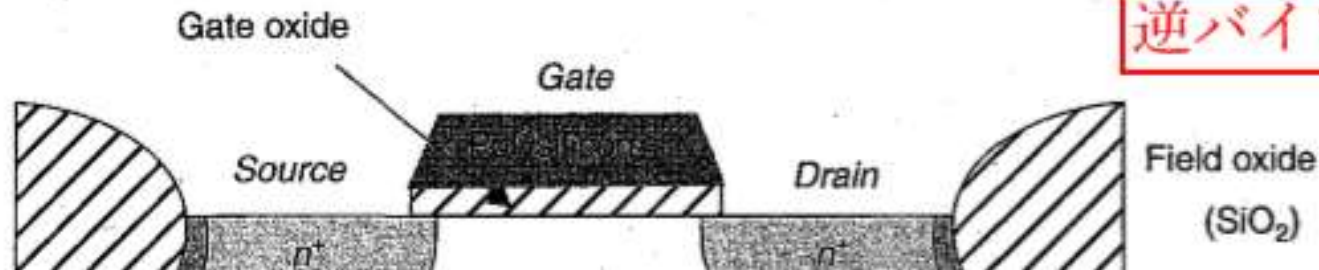


Figure 2.15

Exercise: EX_109-3 p40 [STE-101-207]

- At the most superficial level ~ から28行目まで

- Exercise

Answer following questions simply (long if you like 😊).

- EX_109-31 What stands for NMOS, PMOS and CMOS?
- EX_109-32 Do you think can we make CMOS circuit by (bipolar) transistors?
- EX_109-33 Why do you think so?
- Due date : Wednesday

EX_109-3 p40 [STE-101-207]

- At the most superficial level, the NMOS transistor can be considered to act as a switch. When a voltage is applied to the gate that is larger than a given value called the threshold voltage V_T a conducting channel is formed between drain and source. In the presence of a voltage difference between drain and source, current flows between the two. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the channel resistance and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.
- In an NMOS transistor, current is carried by electrons moving through an n-type channel between source and drain. This is in contrast with the pn-junction diode, where current is carried by both holes and electrons. MOS devices can also be made by using an n-type substrate and p+ drain and source regions. In such a transistor, current is carried by holes moving through a p-type channel. Such a device is called a p-channel MOS, or PMOS transistor. In a complementary MOS technology (CMOS), both devices are present. In a pure NMOS or PMOS technology, the substrate is common to all devices and invariably connected to dc power supply voltage. In CMOS technology, PMOS and NMOS devices are fabricated in separate isolated regions called wells that are connected to different power supplies. Figure 2.16 shows a cross-section of a CMOS device, where PMOS transistors are implemented in a n-type area embedded in a p-type substrate. For obvious reasons, such a fabrication approach is called an n-well technology.

Figure 2.15 Cross section of NMOS transistor.

閾値電圧

断面図

変調

EX_109-3 p40 [STE-101-207]

At the most superficial level, the NMOS transistor can be considered to act as a switch. When a voltage is applied to the gate that is larger than a given value called the *threshold voltage* V_T , a conducting channel is formed between drain and source. In the presence of a voltage difference between drain and source, current flows between the two. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the channel resistance and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.

正孔と電子

相補的

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電源

組み込み

Circuit symbols for the various MOS transistors are shown in Figure 2.17. In 2008

Memo

フォローアップURL (Revised)

<http://mikami.a.la9.jp/meiji/MEIJI.htm>

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