Science and Technology English I II

Exercise 13 Meiji University

EX1_Day13.pptx 9 Slides June 17th.,2019

http://mikami.a.la9.jp/mdc/mdc1.htm

Renji Mikami

Renji_Mikami(at_mark)nifty.com [mikami(at_mark)meiji.ac.jp]

Day 13 Exercise

2 グループで課題を進める(グループA/Bを明記すること)

- Aグループ はなるべく英文で書く
  - 3-14 :
  - 3-15 :
  - 4-14 :
  - 4-15 :
- Bグループは日本文で書いてもよい
  - 3-14 :
  - 3-15 :
  - 4-14 :
  - 4-15 :

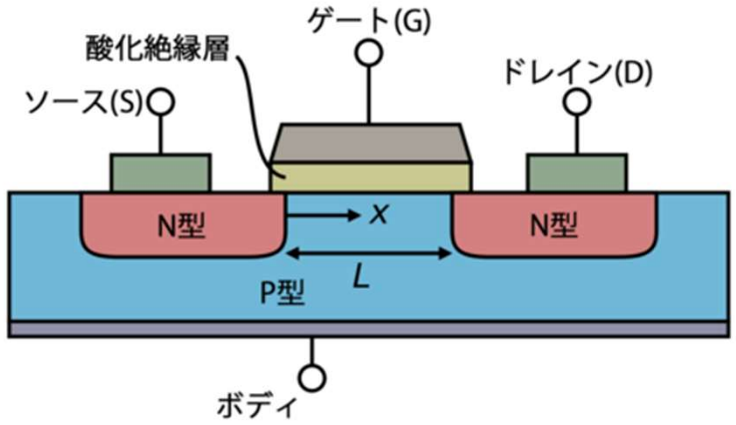
MOS FET

ゲート･ソース間電圧 V_{GS} を変化させるとドレイン電流 I_D が変化する。

N チャンネルタイプは、V_{GS}が高くなるとI_Dが増加する(エンハンスメント型)

P チャンネルタイプは、V_{GS}が高くなるとがI_D減少する(デプレッション型)

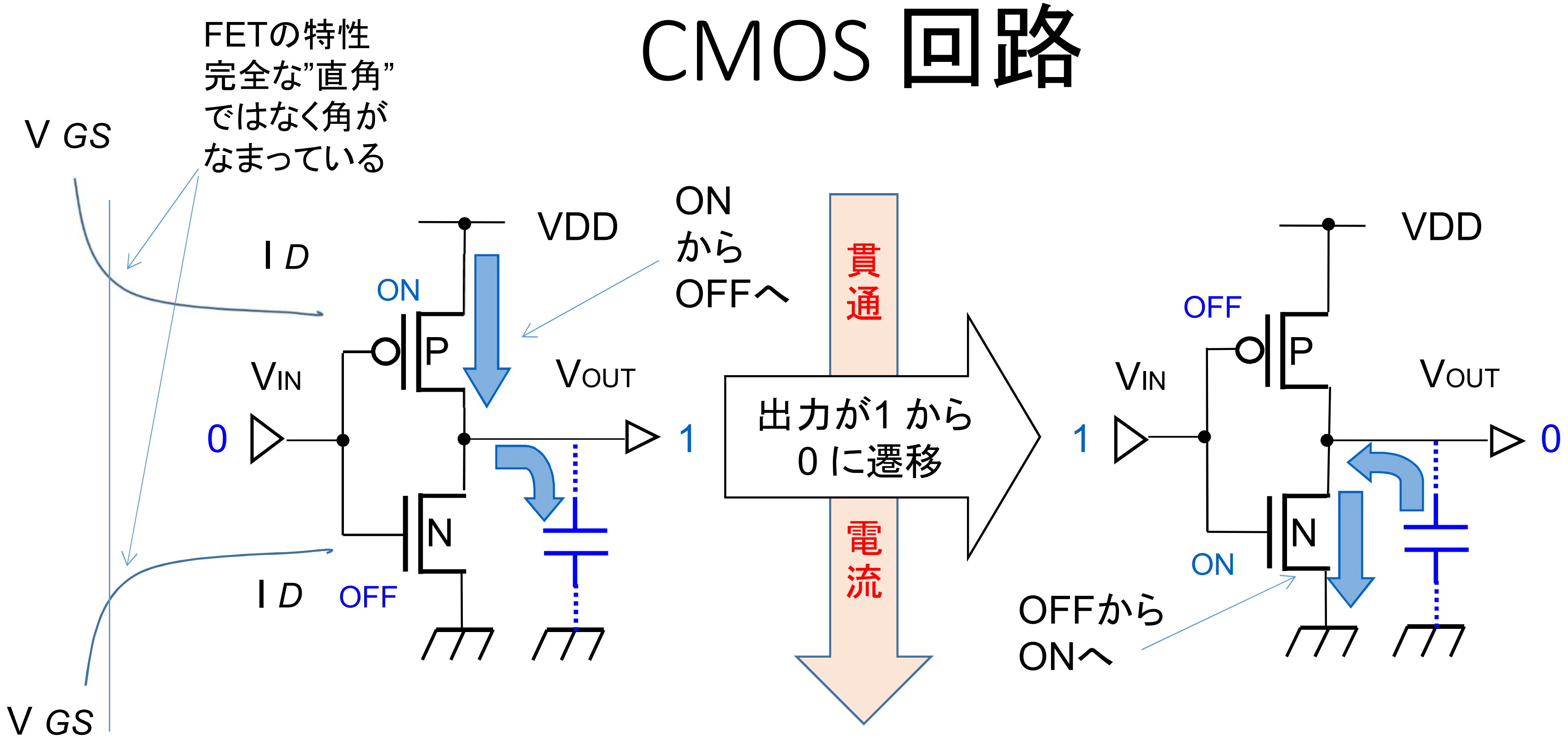
N 型とP 型を組み合わせた回路がCMOS(Complementary MOS)



図版引用:ウィキペディア
https://ja.wikipedia.org/wiki/MOSFET

トランジスタ 回路との比較
トランジスタでは、I_B ベース電流(ベース･エミッタ電流)でI_C コレクタ電流(コレクタ-エミッタ)が変化する。この比がh_{FE} 直流電流増幅率

CMOS 回路



理想動作では、上下のFETは片側はOFFだが、
実際は、双方がONとなり過渡的に電流が流れる

課題文 1 p116 [STE-101-308]から p119 [STE-101-311(3.2.4 Power~)の前まで]]

- ねらい：インバータ の動的特性を読み取る
- *V*は電圧、*I* は電流、下付け添字 *D ドレイン, S ソース, G ゲート*
- (2.51) １１ライン(２ パラグラフ)

Execise1

Answer following questions simply (long if you like ☺).

- 1-1 What stands for V_{DS} and I_D?
- 1-2 What is the (electric) relation between V_{DS} and I_D?

課題文 1-1
p116
[STE-101-308]

3.2.3 Performance: The Dynamic Behavior

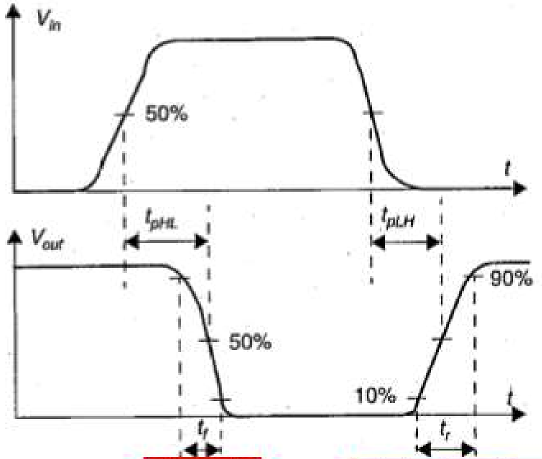
伝播遅延時間

The *propagation delay* t_p of a gate defines how quickly it responds to a change at its input and relates directly to the speed and performance metrics. The propagation delay expresses *the delay experienced by a signal when passing through a gate*. It is measured

伝播遅延

STE-101-309

Figure 3.10 Definition of propagation delays and rise and fall times.



立下り

立ち上がり

between the 50% transition points of the input and output waveforms, as shown in Figure 3.10 for an inverting gate.[1] Because a gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The t_{pLH} defines the response time of the gate for a *low to high* (or positive) output transition, while t_{pHL} refers to a *high to low* (or negative) transition. The overall propagation delay t_p is defined as the average of the two,

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \tag{3.5}$$

Knowledge of t_p is, however, not sufficient to completely characterize circuit performance. The power consumption, noise behavior, and, indirectly, the speed of a gate are also strong functions of the *signal slopes* (as will become clear later in this chapter). This can be quantified with the *rise and fall time* measures t_r and t_f, which are defined between the 10% and 90% points of the waveforms (Figure 3.10).

デファクト標準

課題文 1-2
p117
[STE-101-309]

Knowledge of t_p is, however, not sufficient to completely characterize circuit performance. The power consumption, noise behavior, and, indirectly, the speed of a gate are also strong functions of the *signal slopes* (as will become clear later in this chapter). This can be quantified with the *rise and fall time* measures t_r and t_f, which are defined between the 10% and 90% points of the waveforms (Figure 3.10).

リング

発振器

デファクト標準

The propagation delay of a gate is a function of its fan-in and fan-out. Fan-out gates present an increased load (mostly capacitive) to the driving gate and slow its performance. The increased complexity of a gate due to a large fan-in also has a negative influence on the performance. When comparing the performance of gates in different technologies, it is important not to confuse the picture by including second-order parameters such as fan-in and fan-out. It is therefore useful to find a uniform way of measuring the t_p of a gate, so that technologies can be judged on an equal footing. The de-facto standard circuit for delay measurement is the *ring oscillator*, which consists of an odd number of inverters connected in a circular chain (Figure 3.11). Due to the odd number of inversions, this circuit does not have a stable operating point and oscillates. The period T of the oscillation is determined by the propagation time of a signal transition through the complete chain, or

[1] The 50% definition is inspired the assumption that the switching threshold V_M is typically located in the middle of the logic swing.

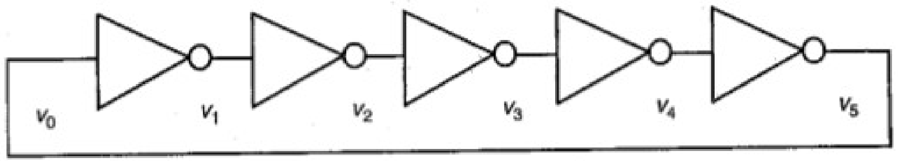
発振する

課題文 1-3
p118
[STE-101-310]

STE-101-310

The period T of the oscillation is determined by the propagation time of a signal transition through the complete chain, or $T = 2 \times t_p \times N$ with N the number of inverters in the chain. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition. Note that this equation is only valid for $2Nt_p >> t_f + t_r$. If this condition is not met, the circuit might not oscillate—one "wave" of signals propagating through the ring will overlap with a successor and eventually dampen the oscillation. Typically, a ring oscillator needs a least five stages to be operational.

阻止する



f（周波数）＝
1／T（周期）

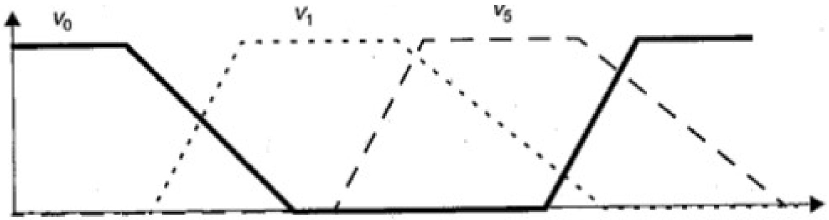


Figure 3.11 Ring oscillator circuit for propagation-delay measurement.

課題文 1-3 p118 [STE-101-310]

無視できない

We must be extremely careful with results obtained from ring oscillator measurements. A t_p of 100 psec by no means implies that a circuit built with those gates will operate at 10 GHz. The oscillator results are primarily useful for quantifying the differences between various manufacturing technologies and gate topologies. The oscillator is an idealized circuit where each gate has a fan-in and fan-out of exactly one and parasitic loads are minimal. In more realistic digital circuits, fan-ins and fan-outs are higher, and interconnect delays are non-negligible. The gate functionality is also substantialy more complex than a simple invert operation. As a result, the achievable clock frequency on average is 50 to a 100 times slower than the frequency predicted from ring oscillator measurements. This is an average observation; carefully optimized designs might approach the ideal frequency more closely.

Example 3.3 Propagation Delay of First-Order *RC* Network

Digital circuits are often modeled as first-order *RC* networks of the type shown in Figure 3.12. The propagation delay of such a network is thus of considerable interest.

課題文 2 p47 [STE-101-214]

構造 成分 分解する 導電チャネル 横方向拡散

MOS Structure Capacitances

The gate of the MOS transistor is isolated from the conducting channel by the gate oxide that has a capacitance per unit area equal to $C_{ox} = \varepsilon_{ox} / t_{ox}$. From the *I-V* equations, we learned that it is useful to have C_{ox} as large as possible, or to keep the oxide thickness very thin. The total value of this capacitance is called the *gate capacitance* C_g and equals $C_{ox}WL$. This gate capacitance can be decomposed into a number of elements, each with a different behavior. Obviously, one part of C_g contributes to the channel charge, and is discussed in a subsequent section. Another part is solely due to the topological structure of the transistor. This component is the subject of the remainder of this section.

位相幾何学

Consider the transistor structure of Figure 2.23. Ideally, the source and drain diffusion should end right at the edge of the gate oxide. In reality, both source and drain tend to extend somewhat below the oxide by an amount x_d, called the *lateral diffusion*. Hence, the effective channel of the transistor L_{eff} becomes shorter than the drawn length (or the length the transistor was originally designed for) by a factor of $2x_d$. It also gives rise to a parasitic capacitance between gate and source (drain) that is called the *overlap capacitance*. This capacitance is strictly linear and has a fixed value

寄生 重ね合わせ

Figure 2.23

Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

担当講師

三上廉司(みかみれんじ)

Renji_Mikami(at_mark)nifty.com

mikami(at_mark)meiji.ac.jp (Alternative)

http://mikami.a.la9.jp/_edu.htm