Science and Technology English I II

Exercise 09 Meiji University

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http://mikami.a.la9.jp/mdc/mdc1.htm

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Day 9 Exercise

2 グループで課題を進める(グループA/Bを明記すること)

- Aグループ はなるべく英文で書く
  - 3-14 :
  - 3-15 :
  - 4-14 :
  - 4-15 :
- Bグループは日本文で書いてもよい
  - 3-14 :
  - 3-15 :
  - 4-14 :
  - 4-15 :

技術解説

周期表 https://www.ptable.com/?lang=ja　4つの力 、価電子、

- 半導体 Si (14ケイ素) Ge(26ゲルマニウム) 4価
- 5価の不純物ドナー(リン、ヒ素など)を加えるとN型半導体(キャリア-電子)に
- 3価の不純物アクセプタ(ホウ素、アルミニウムなど)を加えるとP型半導体(キャリア-ホール)に

課題文 1 p39 [STE-101-206]

- ねらい : MOSFET の概要を読み取る
- 2.3 The MOS(FET) Transister
- 9ライン(2 パラグラフ)

Execise1

Answer following questions simply (long if you like ☺).

- 1-1 What is the major advantage of MOS FET?
- 1-2 We focus what in this section?

課題文 1 p39 [STE-101-206]

2.3 The MOS(FET) Transistor

金属-酸化物-半導体 電界効果 製造プロセス・工程

The metal-oxide-semiconductor field-effect transistor (MOSFET or MOS, for short) is certainly the workhorse of contemporary digital design. Its major assets are its integration density and a relatively simple manufacturing process, which make it possible to produce large and complex circuits in an economical way.

静的な、定常的 動的な、過渡的

We restrict ourselves in this section to a general overview of the device and its parameters, as we did for the diode—after a generic overview of the device, we present an analytical description of the transistor from a static (steady-state) and dynamic (transient) viewpoint. The discussion concludes with an enumeration of some second-order effects and the introduction of the SPICE MOS transistor models.

列挙 2次効果

課題文 2 p39 [STE-101-206]-p40[-207]

- ねらい: MOSFET の構造を技術的に読み取る
- 2.3.1 A First Glance at the Device
- 8ライン

Figure 2.15

Exercise

Answer following questions simply (long if you like ☺).

- 2-1 Channels are separated (insulated) by what?
- 2-2 What conductive material is commonly used?
- 2-3 What do you think about the major difference between transistor and FET?

課題文 2 p39 [STE-101-206]

2.3.1 A First Glance at the Device

注入or拡散

シリコン酸化膜

断面図

基板

A cross section of a typical *n*-channel MOS transistor (NMOS) is shown in Figure 2.15. Heavily doped *n*-type *source* and *drain* regions are implanted (or diffused) into a lightly doped *p*-type substrate (often called the *body*). A thin layer of silicon dioxide (SiO_2) is grown over the region between the source and drain and is covered by a conductive material, most often polycrystalline silicon (or polysilicon, for short). The conductive material

多結晶

導電性材料

絶縁

forms the *gate* of the transistor. Neighboring devices are insulated from each other with the aid of a thick layer of SiO_2 (called the *field oxide*) and a reverse-biased *np*-diode, formed by adding an extra p^+ region, called the *channel-stop implant* (or *field implant*).

逆バイアス電圧

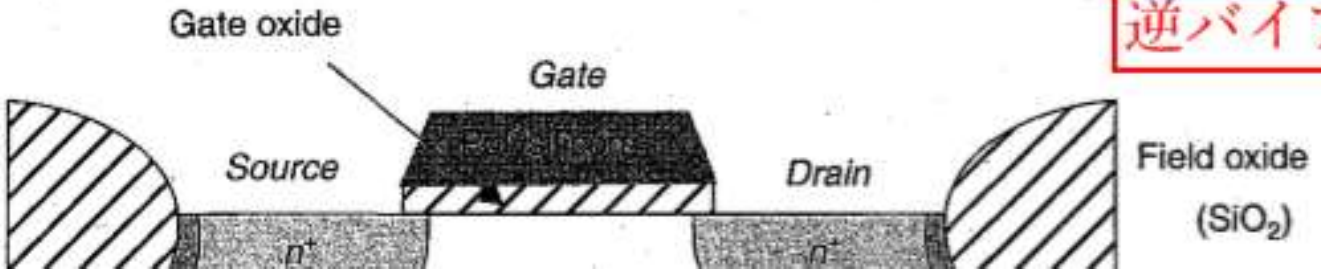

Figure 2.15

課題文 3 p40 [STE-101-207]

- At the most superficial level ~　から28行目まで
- Exercise

Answer following questions simply (long if you like ☺).

- 3-1 What stands for NMOS, PMOS and CMOS?
- 3-2 Do you think can we make CMOS circuit by (bipolar) transistors?
- 3-3 Why do you think so?

Figure 2.15 Cross section of NMOS transistor.

閾値電圧

断面図

変調

At the most superficial level, the NMOS transistor can be considered to act as a switch. When a voltage is applied to the gate that is larger than a given value called the *threshold voltage* V_T, a conducting channel is formed between drain and source. In the presence of a voltage difference between drain and source, current flows between the two. The conductivity of the channel is modulated by the gate voltage—the larger the voltage difference between gate and source, the smaller the channel resistance and the larger the current. When the gate voltage is lower than the threshold, no such channel exists, and the switch is considered open.

正孔と電子

相補的

In an NMOS transistor, current is carried by electrons moving through an *n*-type channel between source and drain. This is in contrast with the *pn*-junction diode, where current is carried by both holes and electrons. MOS devices can also be made by using an *n*-type substrate and p^+ drain and source regions. In such a transistor, current is carried by holes moving through a *p*-type channel. Such a device is called a *p*-channel MOS, or PMOS transistor. In a complementary MOS technology (CMOS), both devices are present. In a pure NMOS or PMOS technology, the substrate is common to all devices and invariably connected to dc power supply voltage. In CMOS technology, PMOS and NMOS devices are fabricated in separate isolated regions called *wells* that are connected to different power supplies. Figure 2.16 shows a cross-section of a CMOS device, where PMOS transistors are implemented in a *n*-type area embedded in a *p*-type substrate. For obvious reasons, such a fabrication approach is called an *n-well* technology.

電源

組み込み

Circuit symbols for the various MOS transistors are shown in Figure 2.17. In gen

Memo

フォローアップURL (Revised)

http://mikami.a.la9.jp/meiji/MEIJI.htm

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