A Wireless Capsule Endoscopic System with a Low-Power Controlling and Processing ASIC

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***Abstract*—This paper presents the design of a wireless capsule endoscopic system with a low-power controlling and processing ASIC. The ASIC aims at several design challenges including system power reduction, system miniaturization and wireless wake-up method. These challenges are met by deploying optimized system architecture, integration of an area and power efficient image compression module, a power management unit (PMU) and a novel wireless wake-up subsystem with zero standby current. The ASIC has been fabricated in 0.18-μm CMOS technology. The achieved performance will be demonstrated with corresponding measurement results. The wireless capsule endoscope prototype base on the ASIC is under development and the demo system will be brought forth soon.**

I. INTRODUCTION

Successive improvements in microelectronics and integration technology have led to the emergence of wireless capsule endoscopic systems [1] which can allow people to study the entire small intestine directly. However, several design challenges still have to be tackled. First, the power budget is limited by the battery. Effective low power techniques have to be employed to ensure long lifetime of the system. Second, as few off-chip components as possible are required for highly-miniature-sized system. Third, an un-touched wake-up means has to be adopted to turn on/off the system after being hermetically encapsulated within the package. In this paper, a wireless endoscopic system with a controlling and processing ASIC is presented, for which the aforementioned challenges were effectively managed.

The paper is organized as follows. Section II presents the wireless capsule endoscopic system architecture. Section III gives the design of the ASIC in detail. Section IV describes the implementation and test results. The conclusion is summarized in section V.

II. DESIGN OF WIRELESS CAPSULE ENDOSCPIC SYSTEM

The proposed wireless capsule endoscopic system is composed of a digital-analog mix mode ASIC together with a commercial CMOS image sensor and an ultra-low-power RF transceiver, as shown in Fig. 1. The image sensor provides images with VGA resolution at 30fps. The image data would be processed by the ASIC which is composed of a digital baseband processing unit, a power management unit (PMU) and a wireless wake-up subsystem. The ASIC also controls a 433MHz RF transceiver which features with FSK modulation, 200kbps raw data rate and only 5mA current consumption in continuous TX/RX mode. The system is powered by two 1.5V lithium batteries connected in series except the wireless powered wake-up subsystem.

Once the system is activated by the wake-up subsystem, the integrated PMU has to not only supply on-chip functional blocks but also deliver the power for CMOS image sensor, RF transceiver and illumination LEDs. The clock is also provided by the on-chip oscillator in PMU. Bidirectional communication protocol implemented in the program ROM facilitates the control of the capsule such as changing image size or system status. Image compression is also introduced to reduce both the overall power dissipation and the transmission bandwidth. The compressed data would be received by the data recorder. Finally, the received data would be decompressed and displayed on PC.

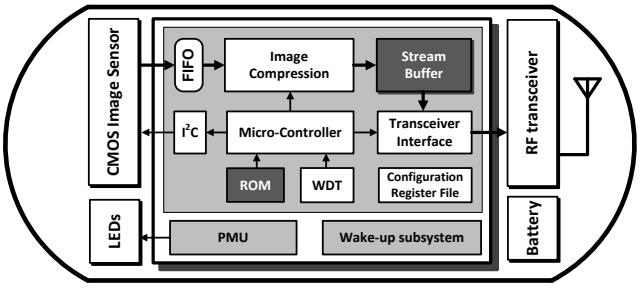

Fig. 1. System architecture of wireless endoscopic system

III. DESIGN OF LOW-POWER CONTROLLING & PROCESSING IC

A. System Architecture of the ASIC

One of the primary design targets of battery-operated medical device is power reduction. Measurement result shows that a great fraction of the battery current is consumed by the RF transceiver of which the power dissipation is difficult to optimize. Instead, an architecture level low-power technique, image compression, is introduced in the baseband processing unit to reduce the

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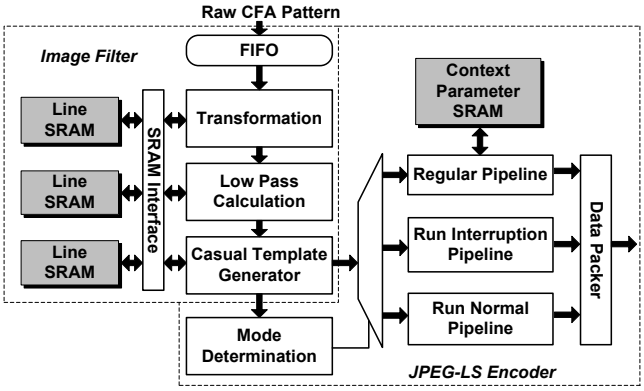

Fig. 2. Block diagram of image compression

data mount and associated RF energy. Though image compression itself would cause extra power consumption, compared to the saved RF energy, the overall power reduction can be achieved.

Unlike the previous architecture based on FSM [2], the proposed architecture is mainly composed of a micro-controller and hardware accelerators. The micro-controller is dedicated to run software that implements high-level communication protocol and flow control. Low-level physical computation is efficiently done by specific hardware accelerator which is better in terms of power consumption and processing time.

B. Area and Power Efficient Image Compression module

The integrated image compression module is dedicated developed for Bayer color filter array (CFA) pattern of CMOS image sensor with great concern of area and power efficiency. The block diagram is shown in Fig. 2. It is mainly composed of an image filter and a standard JPEG-LS encoder [3]. The VLSI-oriented image filter algorithm derived from [4] acts as a preprocessing step for JPEG-LS encoder. It performs pixel transformation and low-pass filtering calculation to depress the high spatial frequencies so as to promote the compression ratio of the following JPEG-LS encoder. JPEG-LS is an established standard for lossless compression, which provides both the highest lossless compression ratio and the fastest compression speed for medical images.

To get an area and power efficient VLSI implementation of JPEG-LS encoder, the data path has been optimized for minimum resource utilization and power consumption. Three parallel three-stage pipelines are designed separately for regular mode, run interruption state and run normal state, as shown in Fig. 3. Each stage is allocated with four clock cycles. For each pixel, only one pipeline is activated by the mode determination unit, which avoids the unnecessary computation of the other two pipelines and leads to considerable power reduction. Experiment has shown that independent data path for different modes and states can cause an average of 45% power reduction, especially for flat images, because most pixels will be processed by Run-

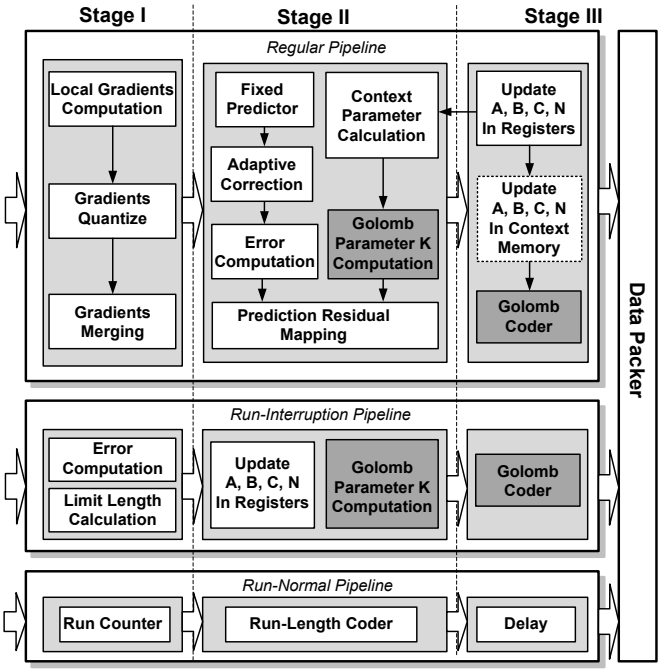

Fig. 3. Data path of JPEG-LS encoder

Normal pipeline with very simple computation. In addition, in-stage resource sharing is extremely exploited between pipelines for common computation such as Golomb parameter k in the second stage and Golomb coder in the third stage, as shown in the dark gray color in Fig. 3.

A two-level hierarchy memory access method is proposed to eliminate unnecessary memory accesses in the process of context parameters (A, B, C, N) updating. In the proposed method, the context parameters are firstly cached in registers in Regular pipeline. The context memory will be accessed only if the next pixel belongs to a different context model, otherwise the value of registers will be used for accumulation without memory access, as shown in Fig.4. Hence the update of context memory only activates when the quantized context changes which cause an average of 52% reduction of the number of memory access. This results in obvious reduction of associated power dissipation.

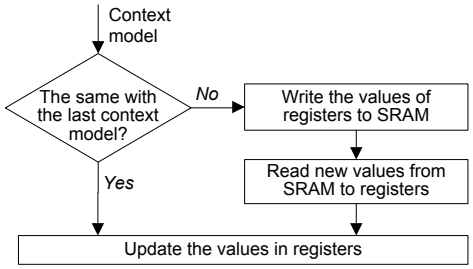

Fig. 4. Memory accesses reduction method of JPEG-LS encoder

C. Power Management Unit (PMU)

The miniature size requirement of wireless endoscopic system makes very severe demand on the area of PCB board as well as the number of on-board components. The integration of PMU allows one to reduce the on-board

components and PCB routing area. The block diagram of PMU is shown in Fig. 5.

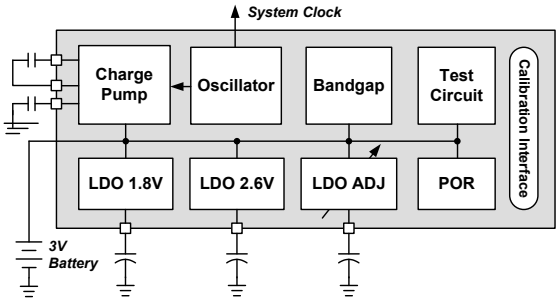

Fig. 5. Block diagram of integrated PMU

The 3.3 maximum operating voltage of the 0.18-μm CMOS technology facilitates the design of LDO which regulates the battery voltage 3V down to a desired output voltage. The LDO can be directly powered by battery without over-voltage problem. Fig. 6 illustrates the LDO circuitry design derided from [5]. It is composed of an error amplifier (M1~M8), a unit-gain buffer (M9~M12), a PMOS pass device, a feedback network (R1, R2) and off-chip loading capacitance C_L.

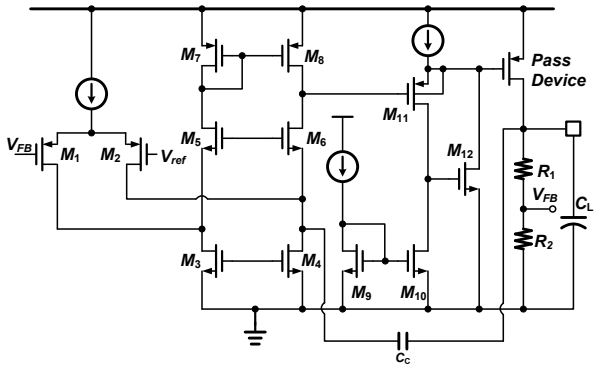

Fig. 6. Schematic of LDO

Illumination LEDs need a constant voltage higher than the battery voltage to provide constant light density. This is achieved by the integrated charge pump, as shown in Fig. 7. M_1, M_4, M_2, M_3 and the off-chip capacitances C_{fly}, C_L form a voltage doubler which could generate twice of V_{BAT} at node C. A comparator is used for regulating the output voltage to a desired value. To save the energy, two different operating modes are implemented. When strobe signal is active, the charge pump works in high speed mode with high clock frequency and bias current, which results in large output current sourcing ability. Otherwise, low clock frequency and bias current are employed to sustain the output voltage.

The clock of charge pump and the digital core is generated by a fully integrated on-chip oscillator. The reference voltage is generated by bandgap reference.

D. Wireless wake-up subsystem

A RFID-like wireless wake-up subsystem is integrated to replace the conventional dry reed switch. It can wirelessly

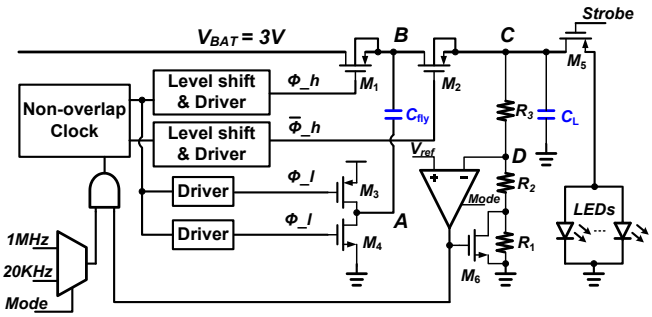

Fig. 7. Schematic of charge pump for driving LEDs

enable/disable the system or to make a configuration of the system after being hermetically encapsulated within the package.

The function blocks in the wake-up subsystem are shown in Fig. 8. The energy recovery block converts part of the incoming RF signal power to a dc voltage (VRF) which supplies all active circuits. The clock and data recovery (CDR) block recovers a digital signal from the received RF signal with amplitude shift keying (ASK) modulation, and generates a synchronous clock signal. The identification and command recognition (ICR) block compares the received device identification code with the desired value and then recognizes valid switching command. After that, the ICR block generates enable/disable signal through level shifter to the PMU. Therefore, the wireless endoscopic system can be wireless enabled/disabled without extra power consumption.

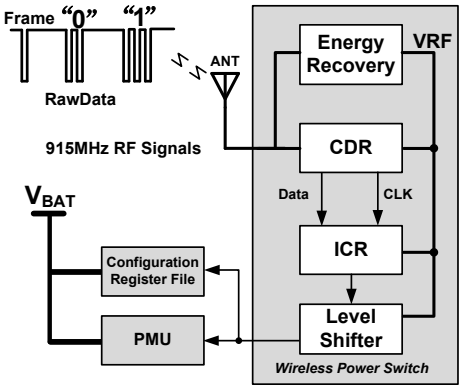

Fig. 8. Blocks diagram of wireless wake-up subsystem

IV. Implementation Results

The digital-analog mix mode ASIC has been fabricated in 0.18-μm 1P6M CMOS technology. The chip layout is shown in Fig. 9 and chip performance is summarized in Table I.

TABLE I. Chip Performance Summary

Technology	0.18-μm 1P6M CMOS
Die size	3.4 mm x 3.3 mm
Supply voltage	3 V
Off-chip components	5 capacitances less than 1μF
Logic gates	23.4 k
Memory	764 kbits (10.2k for image filter, 17.5k for JPEG-LS encoder, 737k for stream buffer)

Clock frequency	20~24MHz (Adjustable)
Image resolution	VGA or QVGA
Compression ratio	3 ~ 4 bpp
Throughput	2 fps for VGA images

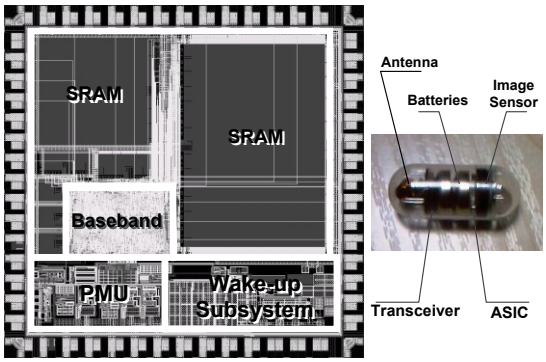

Fig. 9. Chip Layout and the photo of the system prototype

Table II shows a comparison of the proposed implementation of JPEG-LS encoder (without image filter) to other implementations available in academia. It is easily observed that the proposed JPEG-LS implementation presents the lowest gate counts (19.5k) and the lowest memory requirements (17.5kbits).

TABLE II. Comparisons with the other JPEG-LS encoder implementations

	[6]	[7]	[8]	[8]	This work
Year	2005	2002	2007	2007	2008
Technology (um)	UMC 0.18	unknown	TSMC 0.18	TSMC 0.09	UMC 0.18
Resolution (pixels/ line)	640	640	640	640	640
Logic Gates	70 k	49.4 k	28.1 k	25.7 k	19.5 k
Memory (bits)	24 k	32.7 k	20.8 k	20.8 k	17.5 k

The design specifications of the LDO's and the charge pump are shown in table III and table IV, respectively. The start-up waveform of LDOs and charge pump from a previous version implementation is shown in Fig.10.

TABLE III. PERFORMANCE SUMMARY OF LDOS

	1.8V & 1.1V LDO	2.6V LDO	Condition
Vin	3.0V	3.0V	
Load Capacitance	1μF	1μF	
Output current	0~30mA	0~30mA	
Quiescent current	18μA	20μA	No load current
Line regulation	0.25mV	0.14mV	Vin 2.8V~3.2V
Load regulation	1.9mV	2.0mV	I_{Load} 0.1~30mA
Power Supply Rejection	73dB	72dB	Frequency @50kHz
Chip area	0.046mm^2	0.046mm^2	

TABLE IV. PERFORMANCE SUMMARY OF CHARGE PUMP

Mode	Clock	Icontrol	Vout	Voltage Ripple
High speed	1MHz	14μA	4V	50mV@5mA
Low speed	20KHz	4μA	4V	210mV@0mA
Standby	No clk	< 1nA	0V	--

The measurement from a separate prototype IC shows that wireless wake-up subsystem can supply at least 2.7μA current to an external load when received a RF power as low as 60μW. 25kbps data rate can be achieved when receiving commands. The standby current of WWU is always below 10nA.

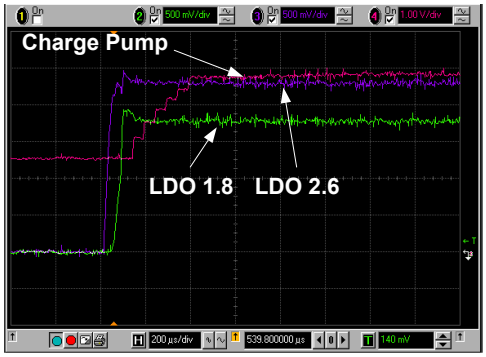

Fig. 10. Start-Up waveforms of LDOs and charge pump (the other blocks are not shown)

A system prototype based on the proposed ASIC is being developed, of which the photo is shown in the right of Fig. 9. The system is encapsulated in the package with the size of Φ11.3mm, length 26.7mm.

V. CONLUSION

This paper presented a wireless endoscopic system with a controlling and processing ASIC, which is composed of a digital baseband module with image compression ability, an integrated power management unit and a wireless wake-up subsystem. The ASIC has been fabricated in 0.18um CMOS technology and a system prototype has been developed on it. Experiment result shows that the ASIC eases the implementation of a low-power miniaturized wireless capsule endoscopic system.

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